(12) UK Patent Application (19) GB (11) 2 289 983 (13) A

(43) Date of A Publication 06.12.1995

(21) Application No 9508294.7

(22) Date of Filing 24.04.1995

(30) Priority Data
(31) 9410973 (32) 01.06.1994 (33) GB
9421289 21.10.1994
9502419 08.02.1995

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(51) INT CL[6]
H01L 27/148

(52) UK CL (Edition N)
H1K KECCX K1EB K4C14
H4F FD18R FD18X FD30A9 FD30K FD83B FGXX
U1S S1031 S2222

(56) Documents Cited
GB 2262383 A GB 2249430 A WO 91/10170 A1

(58) Field of Search
UK CL (Edition N) H1K KECCB KECCX , H4F FCC FGXX
INT CL[6] H01L 27/148 , H04N 1/10 5/14
Online: WPI

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(54) Imaging devices systems and methods

(57) An imaging device 16 comprises a semiconductor substrate including an array of pixel cells 18. Each pixel cell is associated with an individually addressable pixel circuit for accumulating charge resulting from radiation 14, e.g. X-rays incident on a pixel detector. The pixel circuit and the pixel detector can either be implemented on a single substrate, or on two substrates bonded together. An imaging plane can be made up of one imaging device or a plurality of imaging devices tiled to form a mosaic. The imaging devices may be configured as a slot for certain applications, the slit or slot being scanned over the imaging plane. Control electronics 24 can include addressing logic for addressing individual pixel circuits for reading accumulated charge from the pixel circuits. Imaging optimisation can be achieved by determining maximum and minimum charge values for pixels for display, assigning extreme grey scale or colour values to the maximum and minimum charge values and allocating grey scale or colour values to an individual pixel according to a sliding scale between the extreme values. Scattered radiation can be detected and discarded by comparing the detected pixel value to a threshold value related to a minimum detected charge value expected for directly incident radiation and discarding detected pixel values less than said threshold value.

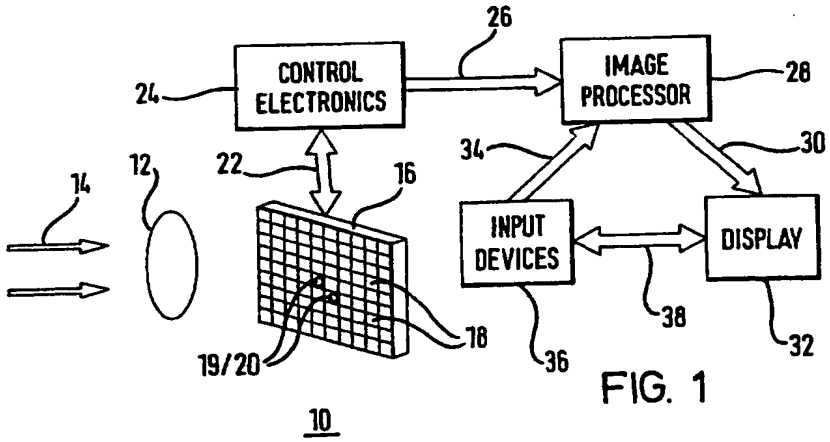


FIG. 1

GB 2 289 983 A

At least one drawing originally filed was informal and the print repr duced here is taken from a later filed formal copy.

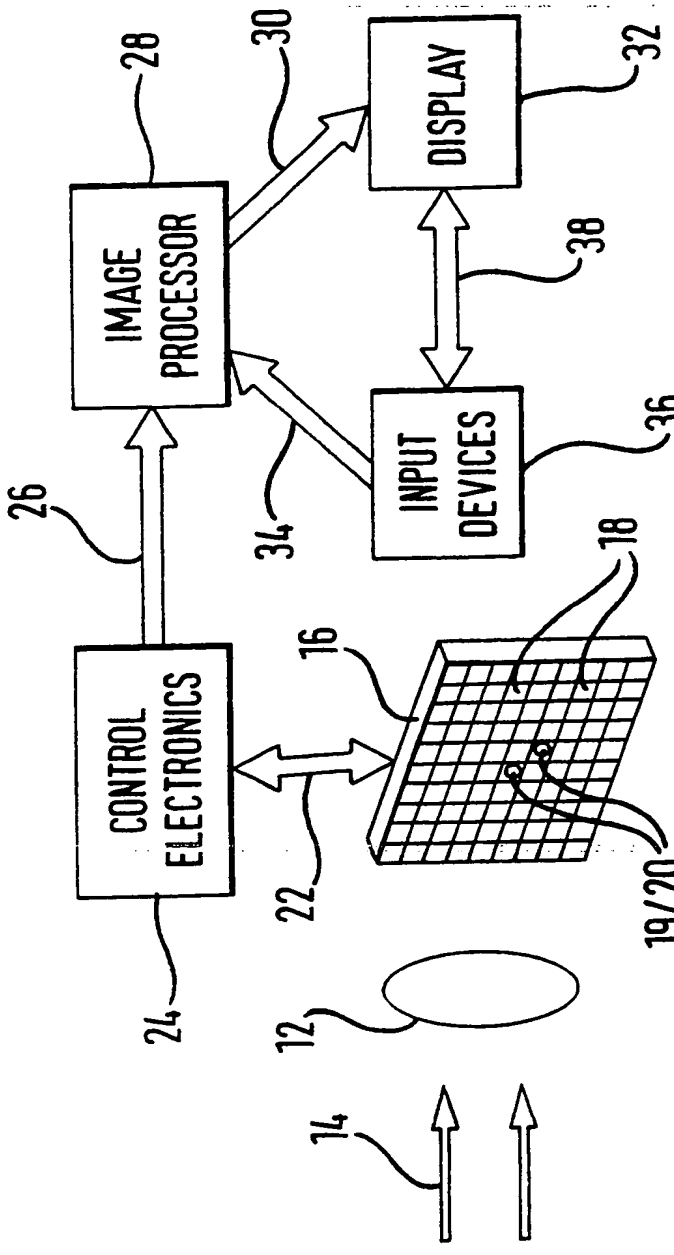


IMAGE PROCESSOR
DISPLAY
INPUT DEVICES
CONTROL ELECTRONICS
10
12
14
16
18
19/20
22
24
26
28
30
32
34
36
38

FIG. 1

FIG. 2

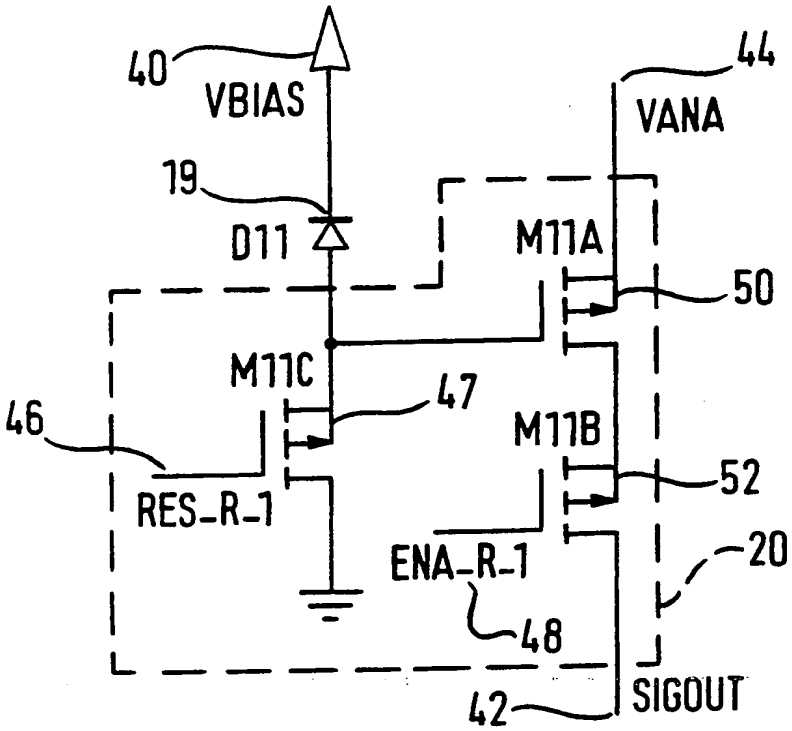
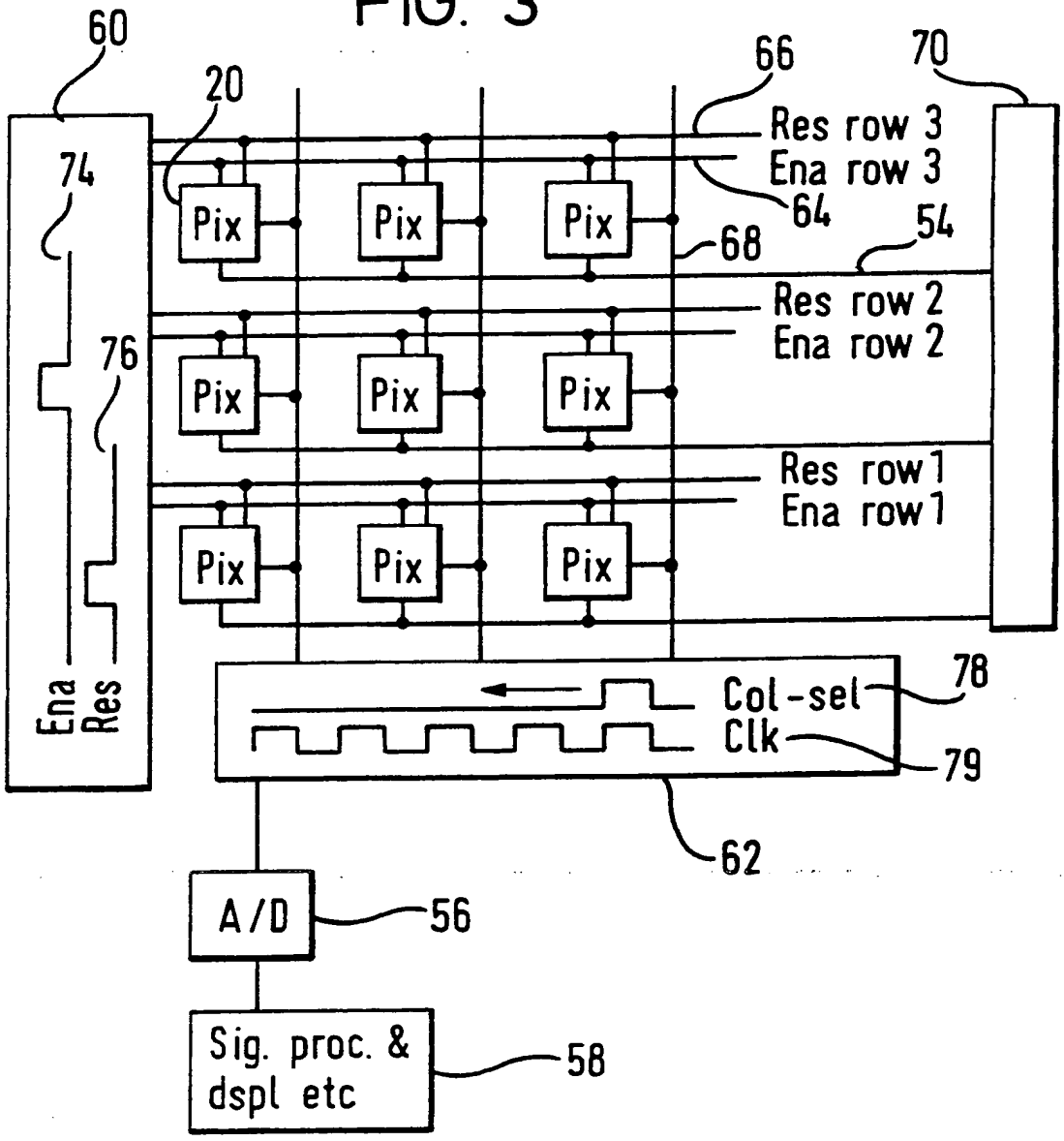

40
VBIAS
44
VANA
19
D11
M11A
50
M11C
47
46
M11B
RES_R_1
52
ENA_R_1
20
48
42
SIGOUT

FIG. 3


60
20
66
70
74
Res row 3
Ena row 3
64
Pix
Pix
Pix
68
54
Res row 2
Ena row 2
76
Pix
Pix
Pix
Res row 1
Ena row 1
Pix
Pix
Pix
Col-sel
78
Clk
79
Ena
Res
62
A/D
56
Sig. proc. &
dspl etc
58

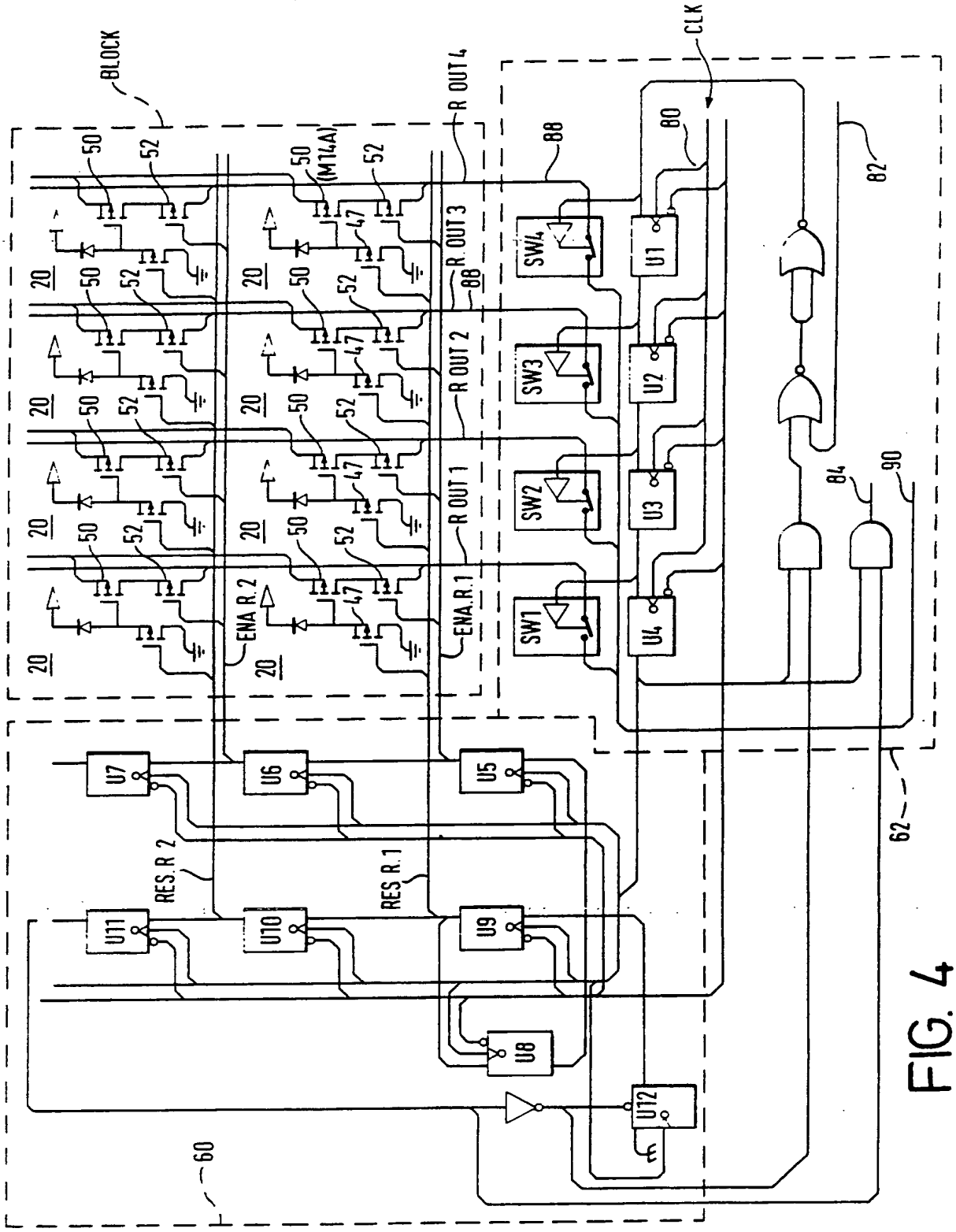

BLOCK
CLK
R OUT 4
R OUT 3
R OUT 2
R OUT 1
ENA R 2
ENA R 1
RES R 2
RES R 1
(M14A)
SW1
SW2
SW3
SW4
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
20
47
50
52
60
62
80
82
84
88
90

FIG. 4

FIG. 5

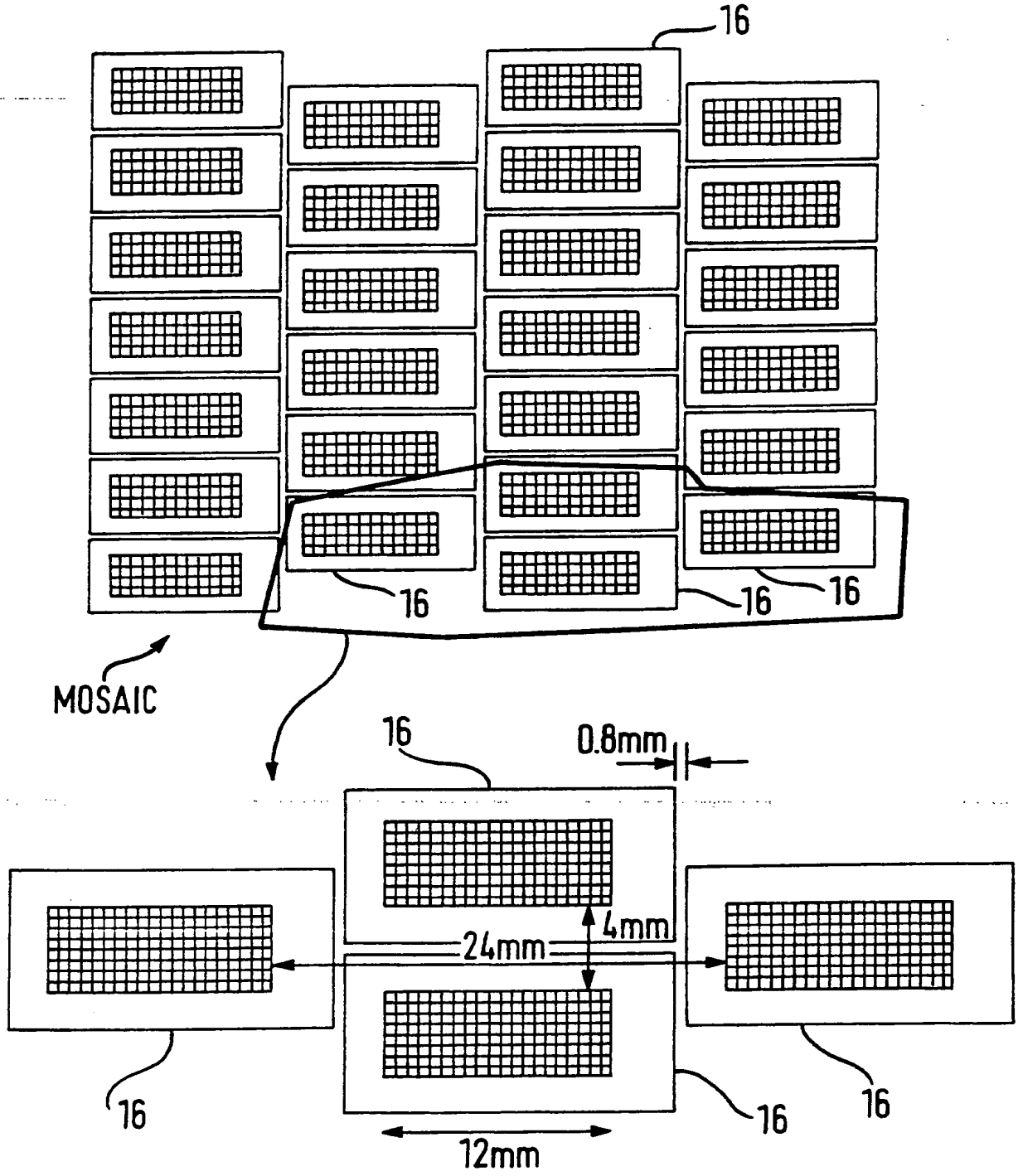


FIG. 5A

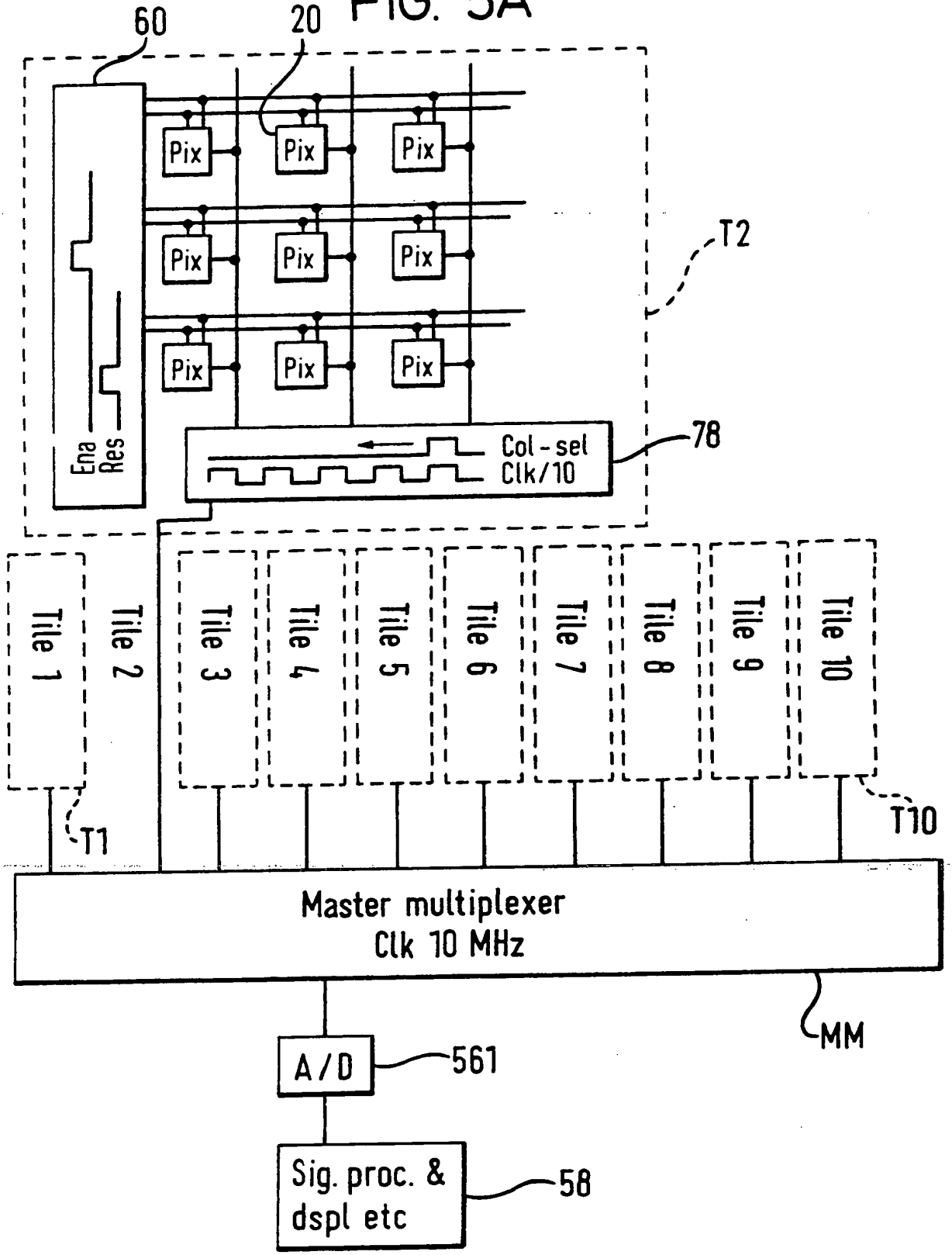

60
20
Pix
Ena
Res
T2
Col - sel
Clk/10
78
Tile 1
Tile 2
Tile 3
Tile 4
Tile 5
Tile 6
Tile 7
Tile 8
Tile 9
Tile 10
T1
T10
Master multiplexer
Clk 10 MHz
MM
A/D
561
Sig. proc. &
dspl etc
58

FIG. 6A

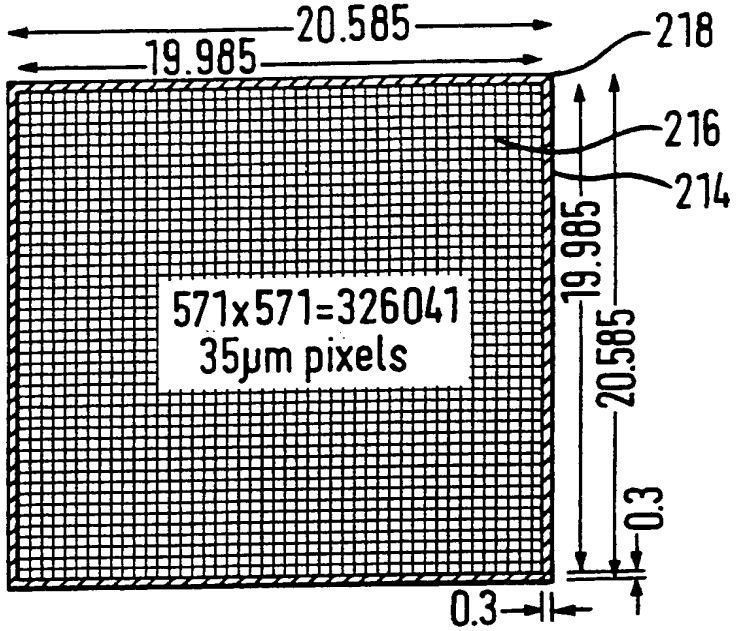


FIG. 6B

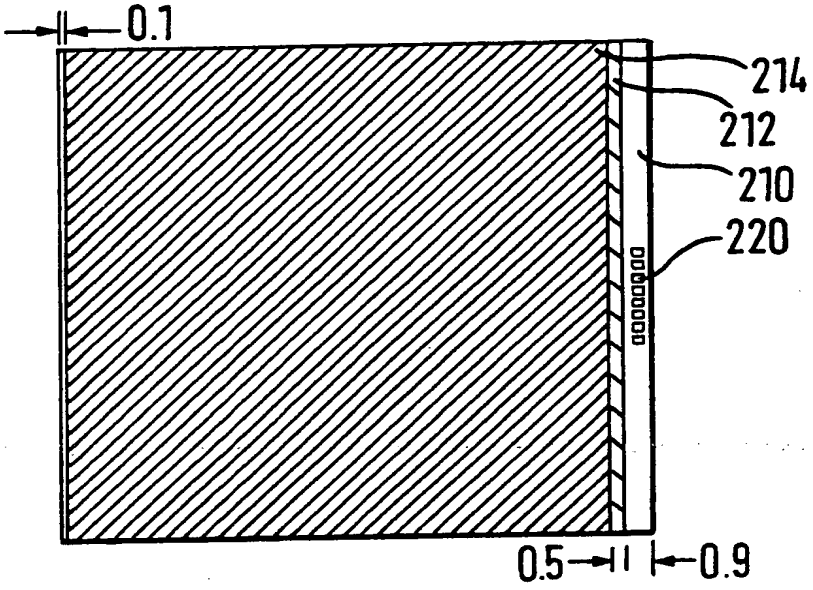


FIG. 6C

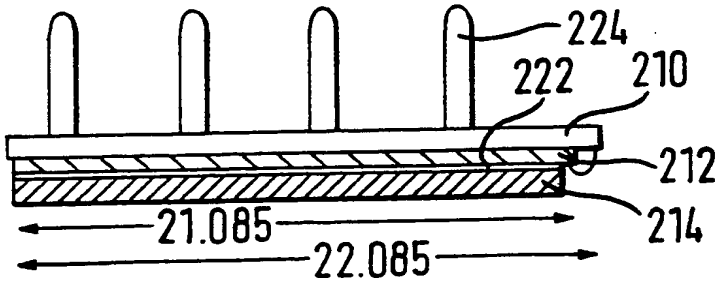
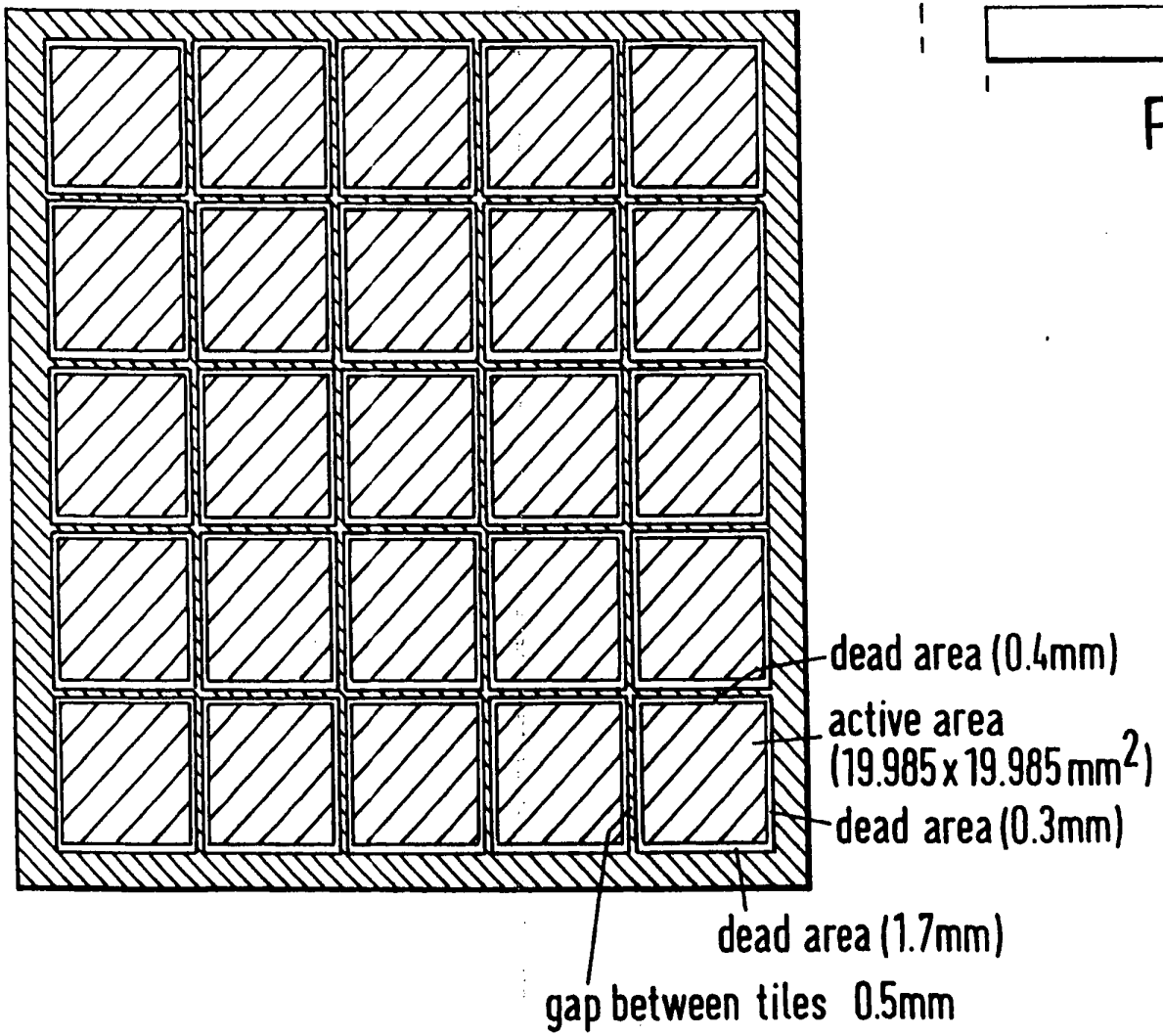


FIG.7A


dead area (0.4mm)
active area
(19.985 x 19.985 mm²)
dead area (0.3mm)
dead area (1.7mm)
gap between tiles 0.5mm

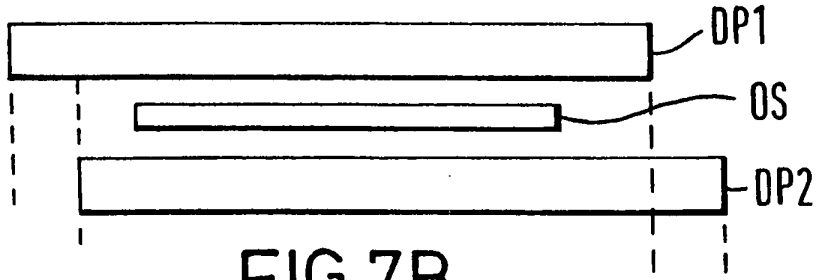

DP1
OS
DP2

FIG.7B

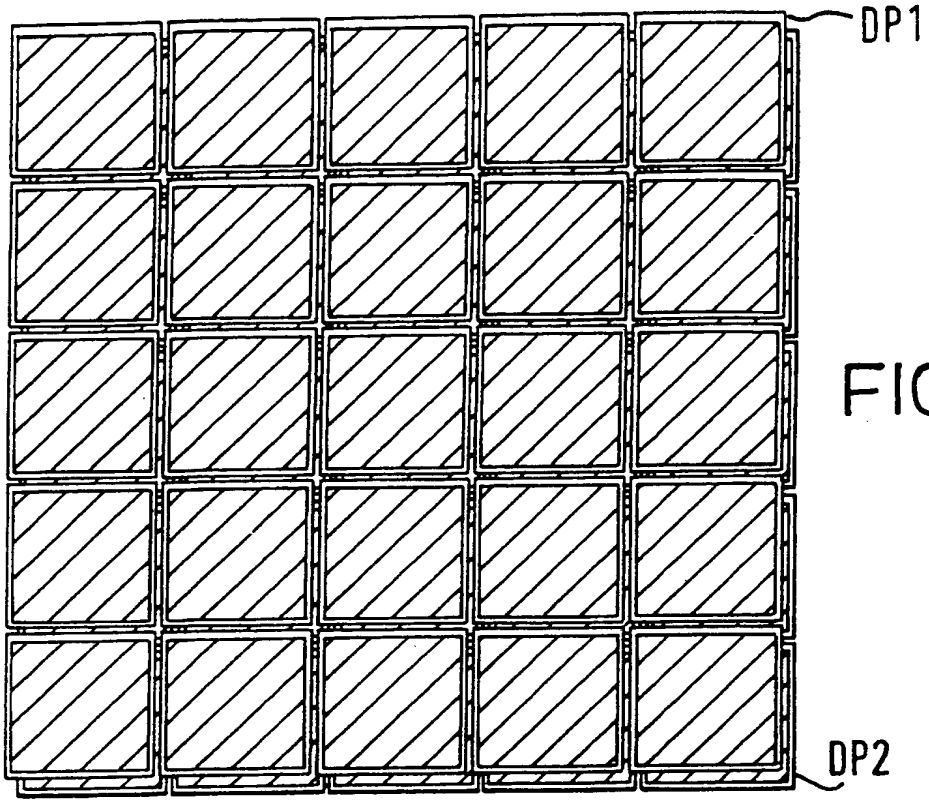

DP1
DP2

FIG.7C

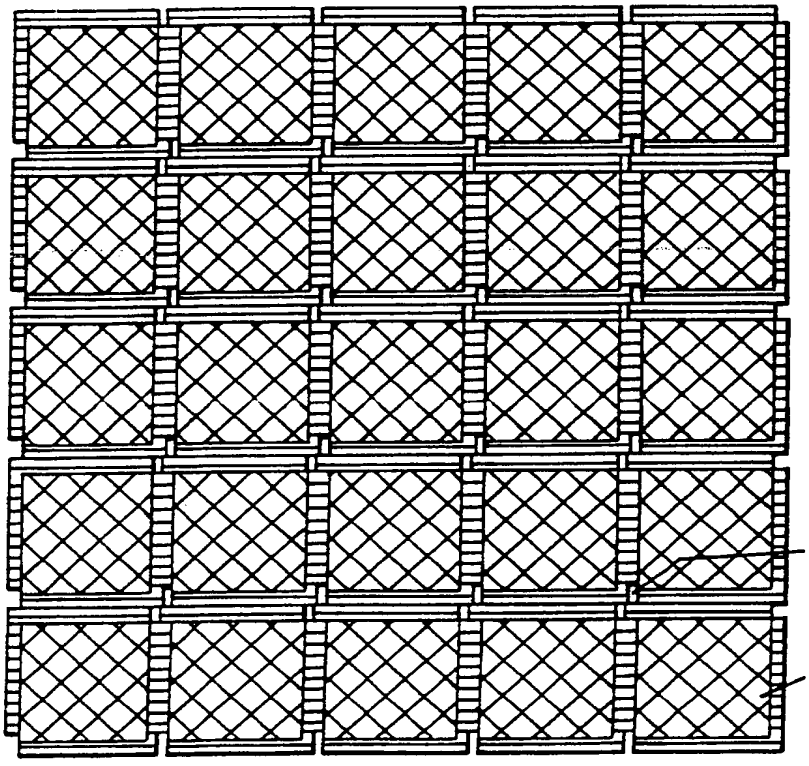

dead spot(1.1mm x 2.6mm)
double detection
18.885mm x(17.385mm)

FIG.7D

FIG. 8

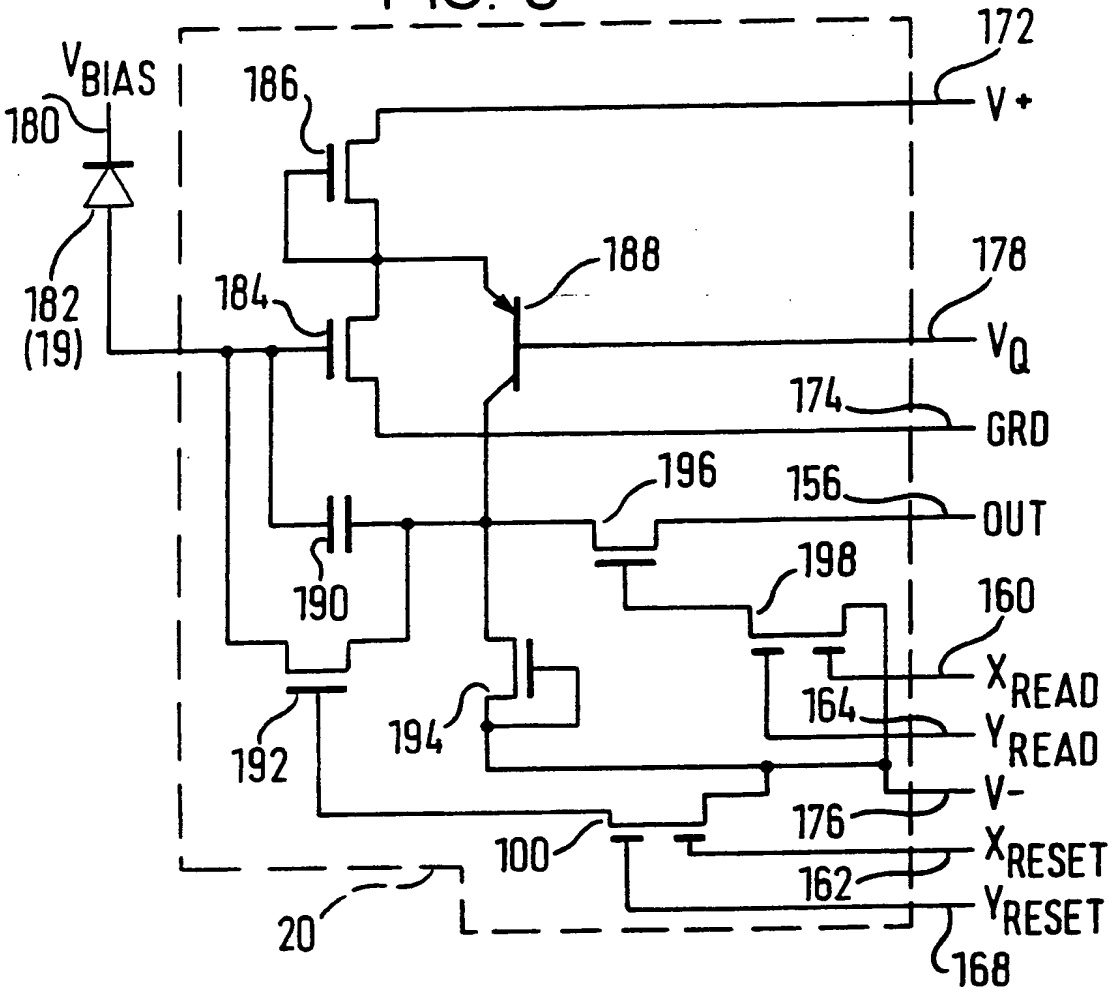

V_{BIAS}
180
182
(19)
186
184
188
190
192
194
196
198
100
20
172
V+
178
V_Q
174
GRD
156
OUT
160
X_{READ}
164
Y_{READ}
V-
176
X_{RESET}
162
Y_{RESET}
168

FIG. 10

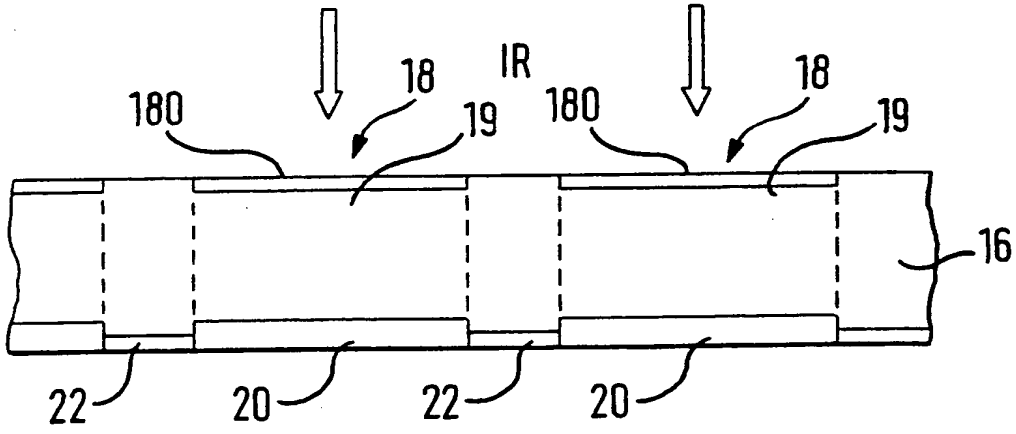

IR
18
18
180
180
19
19
16
22
20
22
20

FIG. 9A

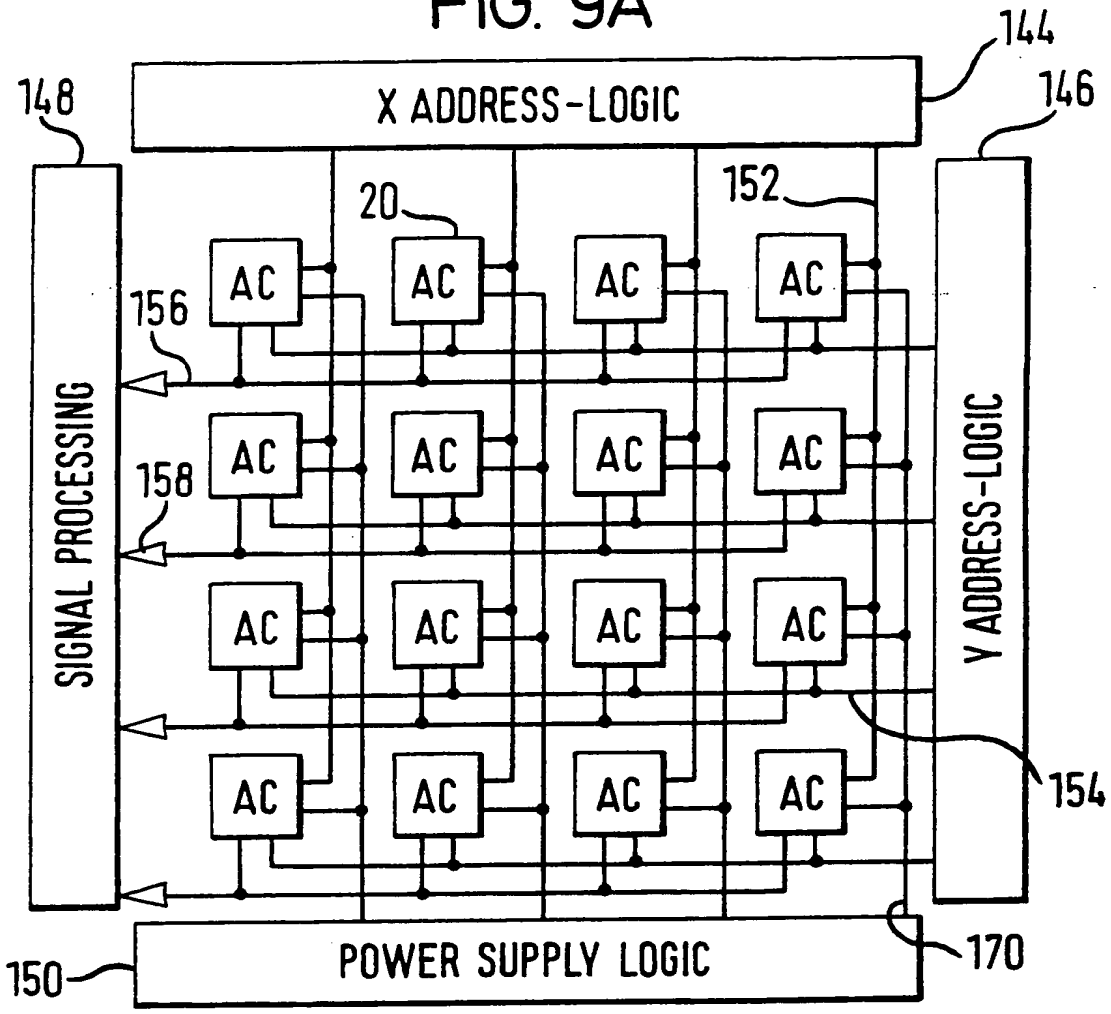

144
X ADDRESS-LOGIC
148
146
152
20
AC
156
158
SIGNAL PROCESSING
Y ADDRESS-LOGIC
154
170
POWER SUPPLY LOGIC
150

FIG. 9B

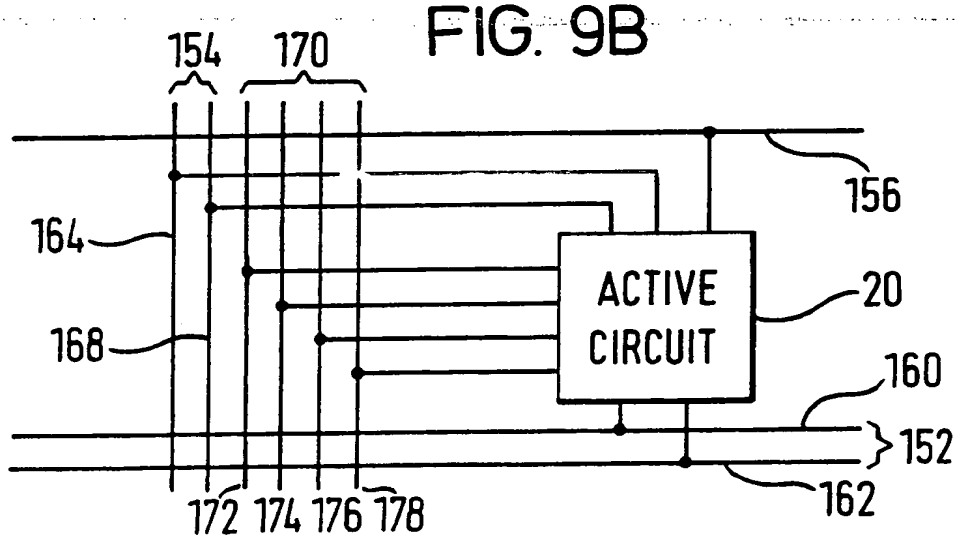
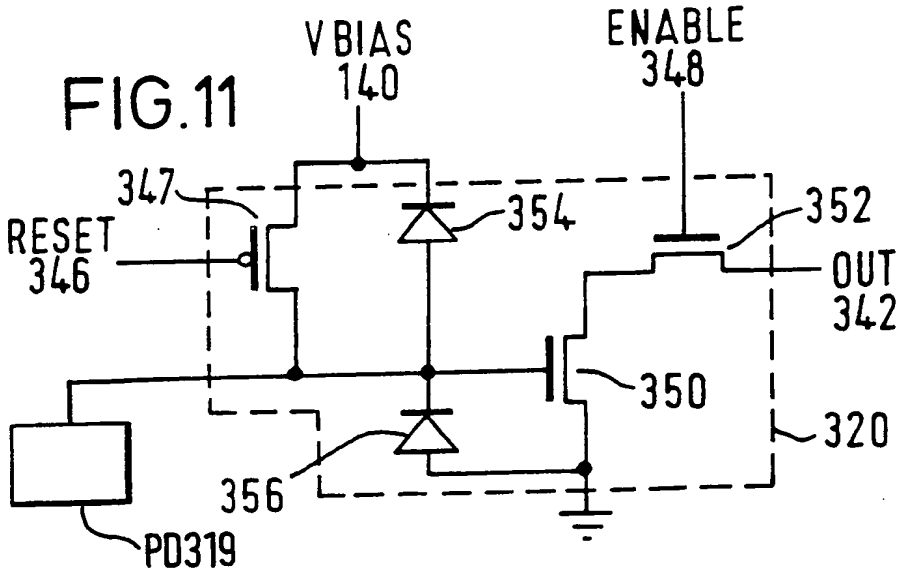

154
170
156
164
ACTIVE CIRCUIT
20
168
160
152
162
172
174
176
178

FIG.11


VBIAS
140
ENABLE
348
347
354
352
RESET
346
OUT
342
350
320
356
PD319

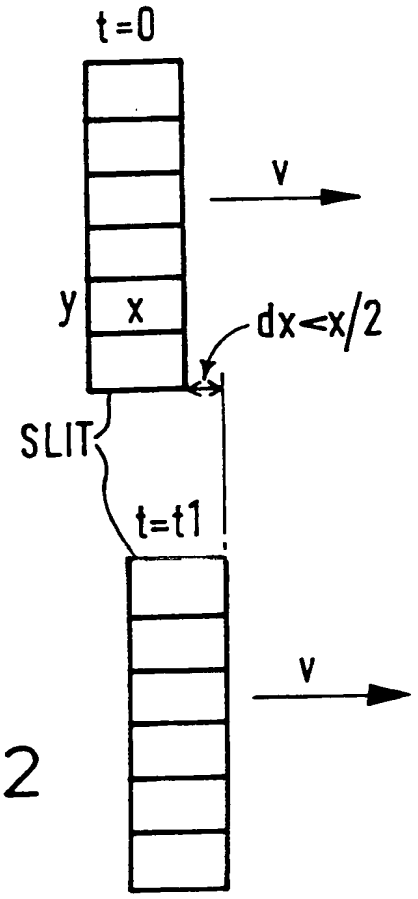

t=0
v
y
x
dx<x/2
SLIT
t=t1
v

FIG.12

Percentage of unscattered photons reaching Si

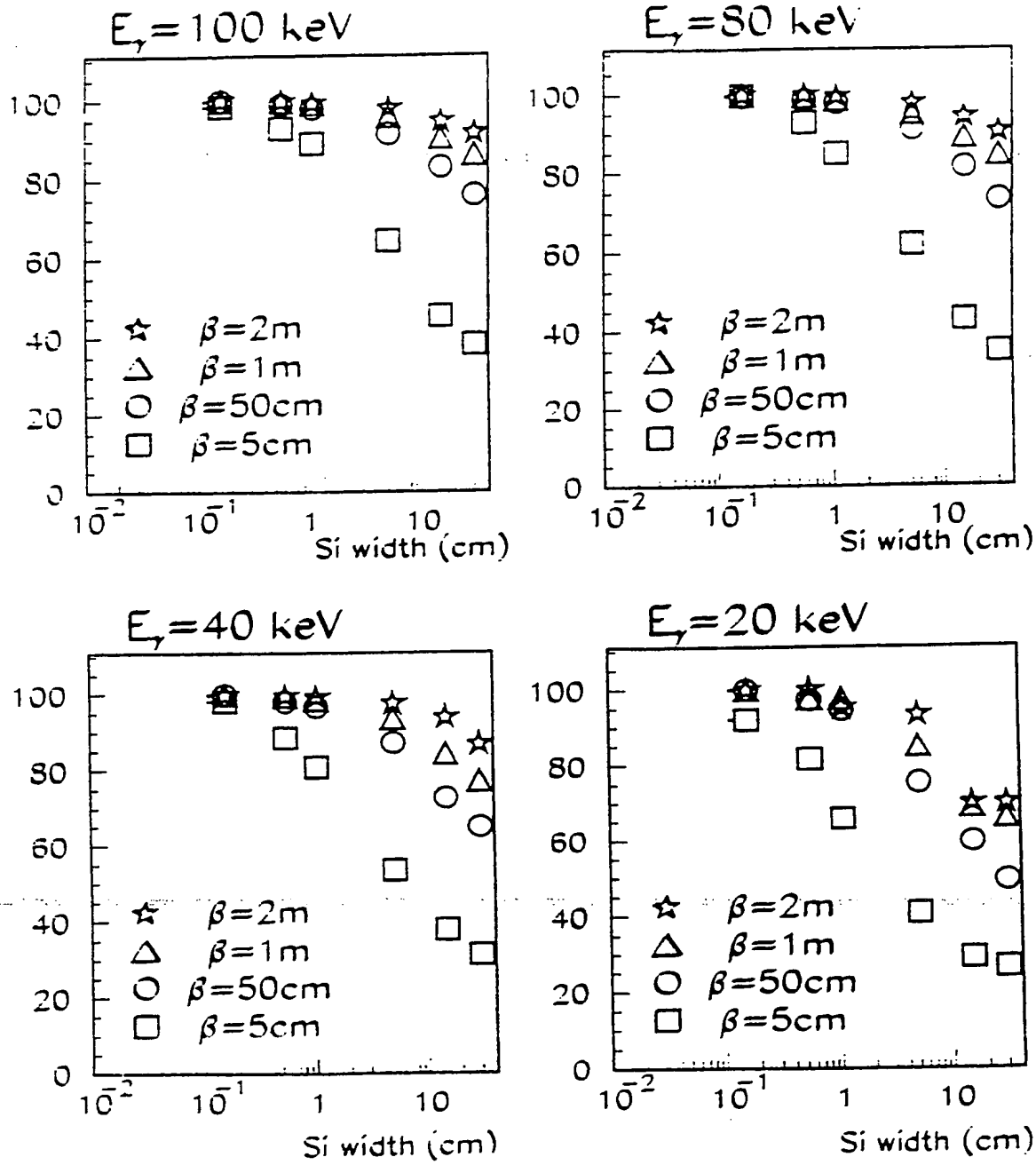


FIG. 13

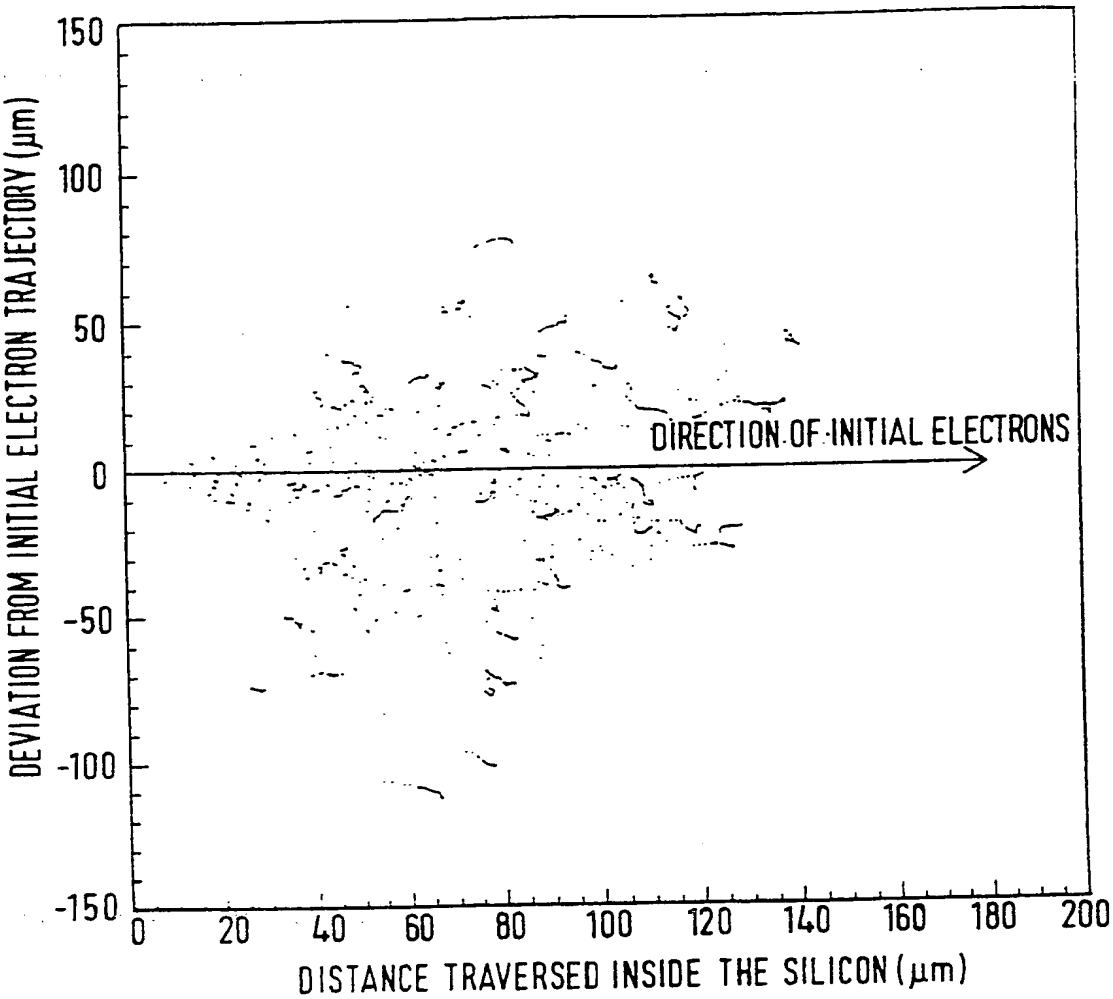

150
100
50
0
-50
-100
-150
0
20
40
60
80
100
120
140
160
180
200
DEVIATION FROM INITIAL ELECTRON TRAJECTORY (μm)
DIRECTION OF INITIAL ELECTRONS
DISTANCE TRAVERSED INSIDE THE SILICON (μm)

FIG.14

2289983

IMAGING DEVICES, SYSTEMS AND METHODS

The invention relates to imaging devices, systems and methods, and in particular to a semiconductor imaging device for use as an image sensor and to an image processing system.

The performance of an imaging system can be assessed, for example, in terms of:

- image resolution, which can be defined by the single point pixel resolution and/or the double point pixel resolution representative of the ability to separate two distinct points;
- imaging efficiency, which can be determined in terms of a dose of radiation needed or the exposure time for generating an image;
- dynamic range, which is related to the ability of an imaging device to record different amounts of radiation of different points without saturation and without destroying the single point resolution (Sufficient dynamic range is particularly important in high intensity applications where there is a large number of incident rays per unit area);
- the response time, image readout speed and image formation speed;
- the analysis, interpretation and storage of images; and
- the imaging area, that is the area of an imaging plane over which an image is collected (In many applications it is important to be able to manufacture large area imaging planes or to design a system for imaging large image areas).

Many different types of imaging devices and systems are known which have differing degrees of performance measured using the parameters listed above for use in differing applications. For example, imaging systems find wide application in medical fields.

Photographic media provide probably the most widely used imaging technique. Photographic media are still widely used in medical applications. Often a photographic medium (e.g. film) is used with a wavelength shifter to increase efficiency, or with digitizers to improve resolution. The photographic film medium does, however, present a number of serious limitations:

- low efficiency (typically 1% if used in isolation);
- poor dynamic range and non-linear response to radiation which

inhibits detection of low contrast objects and can lead to an effective reduction in available resolution;

- passive image recording which limits direct analysis to qualitative analysis (although limited quantitative analysis can be achieved on digitization of the film image).

Conventional photosensitive devices such as photomultipliers and microchannel plates can provide moderate efficiency and resolution (at the millimetre scale).

Also, wire gas chambers can be used for real time imaging with electronic recording of the images. These chambers have excellent efficiency and dynamic range but the resolution is at the 500μm level. High intensity imaging is probably impossible or at best very difficult indeed to achieve as this would require a wire gas chamber which is able to read pulses and reset every microsecond (or less). Under such conditions the chamber would tend to saturate. In addition it is difficult to provide large imaging areas with such chambers because of the presence of the gas which requires continuous pressure and temperature regulation.

Semiconductor components such as charged coupled devices (CCDs) have been used for imaging purposes as well. Surface channel and buried channel devices are the two most commonly used CCDs. A CCD is typically arranged as an array of pixel detector cells, each of which acts as a pixel storage well. Electrodes define a pixel cell and the voltage applied across the pixel cell creates a natural potential well that can store charge, which remains in the semiconductor substrate until it is read out. Examples of CCD imaging devices and systems are described, for example in GB-A-2,262,383 and GB-A-2,249,430.

A CCD is typically operable for imaging low energy optical or ultra-violet radiation. CCD devices can be used for imaging, for example, X-rays. However, in such an application a CCD is typically used in conjunction with a fluorescent screen for converting incident X-rays into optical or ultraviolet wavelengths. The operation of a CCD is such an arrangement can be summarised as follows.

In a first phase, during irradiation, a CCD located behind a fluorescent screen is in a static state and accumulates charge created from photoabsorbed low energy photons from the screen. In a second phase, the charge is clocked through individual pixel cells and

eventually is read out. The transfer of the stored charge from one pixel cell to the next is done by clocking voltages on the pixel cells so that the charge passes from cell to cell in the substrate. The pixel cells themselves do not include any charge storage circuity and the storage capacity of the pixel cells is limited by the capacity of the natural well that is created inside the substrate by applying voltages. Circuitry is provided at the periphery of the CCD and collects the charge after it has been clocked out. Typically, the electron storage capacity of a CCD device is limited to about 700,000 electrons.

A surface channel CCD is a device where the depletion region is a relatively large percentage of the total CCD volume. Interface traps may degrade the transfer efficiency. A buried channel CCD has a relatively small volume which is sensitive to radiation. Both types of CCD have limited storage capacity as mentioned above.

Both types of CCDs are suitable for imaging, for example, low energy X-rays and in such an application, as mentioned above, they are typically used with a fluorescent screen that shifts the incident wavelength to the optical or ultra-violet region. This increases efficiency, but at the same time reduces resolution because of light diffusion.

Thus the CCDs do not directly detect the incident high energy X-rays but are most commonly used with a converting screen. An additional important drawback of CCDs is the readout scheme which allows for ambiguous or 'ghost' hits. This is because the pixels are not accessed in one to one correspondence, but rather they are clocked out. In view of this it is not possible to accumulate multiple frames of an image during the readout procedure.

Developments in the last few years on silicon radiation detectors have made it possible to manufacture single and double sided strip detectors. An example of such a detector is described in UK patent application GB-A-2 265 753. The pitch in these detectors can be quite small thus offering excellent resolution. However for applications with high intensities and/or large imaging areas, for example in mammography, the readout speed would need to be in the GHz region in order avoid ambiguities and 'ghost' hits. Such readout speeds are not realisable, at least not at a realistic cost. When using such devices,

the electronic signals from each strip are read out and the position of the incident radiation is determined. One limitation besides the high readout speed needed is the inability of strip detectors to resolve two incident rays that coincide in time and fall within the pitch of a strip, with the result that it is not always possible unambiguously to resolve a point of incident radiation. As a result of these limitations, the resolution and the efficiency degrades.

Pixel silicon detectors comprise a silicon substrate with electrodes which apply a depletion voltage to each pixel and define a charge collection volume. Simple buffer circuits read out the electric signals when a photon is photo-absorbed or when ionizing radiation crosses the depletion zone of the silicon substrate. The buffer circuits can either be on the same substrate (compare EP-A-0,287,197) as the charge collection volumes or on a separate substrate (compare EP-A-0,571,135) that is mechanically bonded to a substrate having the charge collection volumes in accordance with, for example, the well known bump-bonding technique (bump-bonding is a technique known for a decade or more).

In either case, every time a charge is present as a result of a high energy ray (e.g., 10keV or more), it will be read out and processed. These pixel detectors operate in a pulse mode. The pixel detectors decrease the readout speed needed because there is a higher segmentation and more parallel readout channels. However, they cannot cope with high intensity applications because the readout electronics will overflow thus destroying the image contrast. Besides that, simultaneously incident rays can cause ambiguous and 'ghost' hits that cannot be resolved and worsen the resolution. Although these devices directly detect the incident radiation, they have limitations due to an operation based on a pulse mode and imaging based on the counting of discrete points.

It will be appreciated from the above that all of the devices presently available have limitations which cannot be resolved. Accordingly, an object of the invention is to provide an imaging device based on a different approach which enables the problems of the prior art to be mitigated and/or solved.

In accordance with an aspect of the invention there is provided an imaging device for imaging radiation, the imaging device comprising

an array of pixel cells including a semiconductor substrate having an array of pixel detectors which generate charge in response to incident radiation and a corresponding array of pixel circuits, each pixel circuit being associated with a respective pixel detector for accumulating charge resulting from radiation incident on the pixel detector, the pixel circuits being individually addressable and comprising circuitry for accumulating charge from successive radiation hits on the respective pixel detectors.

The invention provides an imaging device which can be described as an Active-Pixel Semiconductor Imaging Device (ASID). Embodiments of an imaging device in accordance with the invention are suitable, in particular, for high energy radiation imaging such as X-ray, β-ray and α-ray real time imaging.

An ASID is able actively to accumulate charge for individual pixels during irradiation. It directly detects rays incident on a pixel cell detector of the semiconductor substrate and accumulates charge (by accumulating the charge directly as charge values or by converting it to a voltage or current and accumulating the resulting voltage or current) in an active circuit corresponding to the pixel cell detector. By enabling the active circuit for each pixel to be addressed individually (e.g., in random or sequentially order), the stored charge can be read out at any time during or after irradiation.

The active circuit is preferably located proximate to the pixel detector (either integral to the semiconductor substrate integral to the substrate comprising the pixel cell detectors or on a substrate bonded thereto) and has a sufficient dynamic range to accumulate charge corresponding to several hundreds or thousands of radiation hits on the corresponding pixel detector.

Readout of the active pixel circuits can be arranged to occur very rapidly with practically no dead time so that the active circuit and the corresponding pixel cell detector are ready immediately to continue accumulating radiation hits.

Each detecting element and the associated active circuit constitute a randomly accessible, dynamic active imaging pixel capable of storing charge (either directly as charge or as a voltage or current equivalent) during radiation and capable of being read during or after irradiation. The readout speed and the degree of parallel or

sequential signal processing for the read out data can be optimised to match the radiation intensity and the time available to accumulate the image.

Accordingly, an imaging device in accordance with the invention can combine the charge storing abilities of a conventional CCD, but with a higher dynamic range and with the efficiency and speed of a conventional semiconductor pixel detector operating with buffer circuits which do not store charge. Whereas a normal CCD stores charge in a natural potential well, an ASID stores charge (as charge or a voltage or current equivalent) corresponding to many, possibly hundreds and thousands of radiation hits per pixel in active electronic structures associated with respective pixel cell detectors of the pixel detector substrate.

The invention finds particular application for high intensity imaging applications. The problems of unrealistic readout speed, ambiguous and 'ghost' hits of prior pixel detectors and the low efficiency and dynamic range of CCD devices can all be overcome by embodiments of the present invention. However, it will be appreciated that the invention is not limited to high energy and high intensity applications, and that embodiments of the invention can also find application to lower energy applications (e.g., at optical wavelengths) and low intensity applications (in astronomy).

Preferably, each pixel circuit comprises a charge storage device for accumulating charge, for example a capacitor and/or a transistor. In a preferred embodiment of the invention, charge is accumulated on the base of an FET transistor, preferably forming one of a pair of FET transistors connected as a cascode amplification stage.

Preferably also, each pixel circuit comprises circuitry for selectively resetting the charge storage device, for example after readout of any charge stored thereon. A preferred embodiment of the invention comprises a first FET switch responsive to an enable signal to connect the charge storage device to an output line for outputting accumulated charge and a second FET switch responsive to a reset signal to ground the charge storage device to reset the charge storage device.

In some applications, for example gamma cameras and nuclear medicine, the pixel size can be of the order of or less than 1mm across, preferably approximately 350μm across.

In other applications, the pixel cell size can be approximately 150μm across or less, preferably approximately 50μm across or less and more preferably approximately 10μm across with a substrate between 200μm and 3mm thick.

The pixel circuits can be implemented integrally to the substrate and aligned with the corresponding pixel detectors. Alternatively, the pixel circuits can be formed in a further substrate, the further substrate incorporating the pixel circuits being coupled to the substrate incorporating the pixel detectors, with each pixel circuit being aligned with and being coupled to the corresponding pixel detector.

In particular embodiments of the invention, the array comprises a single row of pixel detectors and associated pixel circuits forming a slit-shaped imaging device or a plurality of rows of pixel detectors and associated pixel circuits forming a slot-shaped imaging device. In such an embodiment the pixel circuits for respective pixel detectors can be arranged laterally adjacent to the corresponding pixel detectors.

An imaging system for the imaging device comprises control electronics for the imaging device includes addressing logic for addressing individual pixel circuits for reading accumulated charge from the pixel circuit and selectively resetting the pixel circuit. Preferably, the addressing logic comprises means for connecting output lines of the pixels circuits to an output of the imaging device, means for supplying read enable signals to read enable inputs of the pixel circuits and means for supplying reset signals to reset inputs of the pixel circuits.

The means for connecting output lines can comprise a shift register for sequentially connecting output lines of the pixel circuits for respective columns of pixels to the output of the imaging device. Likewise, the means for supplying read enable signals can comprise a shift register for sequentially supplying read enable signals to read enable inputs of the pixel circuits for respective rows of pixels and/or the means for supplying reset signals can comprise a shift register for sequentially supplying reset signals to reset inputs of the pixel circuits for respective rows of pixels.

Thus, in a preferred embodiment of the invention, the addressing

logic comprises a first shift register for sequentially connecting output lines of the pixels circuits for respective columns of pixels to an output of the imaging device, a second shift register for sequentially supplying read enable signals to read enable inputs of pixel circuits for respective rows of pixels and a third shift register for sequentially supplying reset signals to reset inputs of pixel circuits for respective rows of pixels. The control electronics can include an analogue to digital converter (ADC) for converting charge read from a pixel circuit into a digital charge value.

At least part of the control electronics can be integrated into the semiconductor substrate on which the pixel circuits are formed.

Preferably the imaging system comprising an image processor connected to the control electronics for processing the digital charge values from respective pixel circuits to form an image for display on a display device.

For optimising the display of captured images, the processor determines maximum and minimum charge values for pixels for display, assigns extreme grey scale or colour values to the maximum and minimum charge values and allocates grey scale or colour values to an individual pixel according to a sliding scale between the extreme values in dependence upon the charge value for the pixel.

The grey scale or colour values are preferably allocated in accordance with the following formula:

$$\text{Grey scale value of pixel } i = \text{Min}_{grey} + \frac{(i_{charge} - \text{Min}_{charge})}{(\text{Max}_{charge} - \text{Min}_{charge})} \times (\text{Max}_{grey} - \text{Min}_{grey})$$

In a preferred embodiment of the invention, an imaging system comprising a plurality of imaging devices as defined above is tiled together to form a mosaic. This enables a large area imaging device to be constructed without the yield problems normally experienced with very large surface area integrated devices. The mosaic can comprise a plurality of columns of tiled imaging devices, the imaging devices of adjacent columns being offset in the column direction. Preferably the imaging system includes means for stepping the imaging device to accumulate an image over a complete image area.

In one embodiment, the imaging system comprises two imaging

surfaces, each comprising a mosaic of imaging devices, said imaging surfaces being arranged substantially parallel to one another and spaced from one another with an object to be imaged between said surfaces, the mosaics being offset laterally with respect to one another to give substantially complete imaging of said object. This permits substantially complete imaging in certain applications without the need for translatory mechanisms for the imaging planes.

Respective image outputs of a plurality of tiled imaging devices are preferably connected to a common multiplexer, the output of which multiplexer is connected to a common analogue to digital converter. Also, individual pixel circuits can be addressed for reading accumulated charge at a rate to optimise the resolution of an analogue to digital converter for converting analogue accumulated charge values into digital values. Both of these measures provide design flexibility to optimise between cost (more multiplexing, less ADCs) and image contrast (less multiplexing, more ADCs).

In an imaging system comprising one or more slit- or slot-shaped imaging device(s) as defined above, means can be provided for moving the slit- or slot-shaped imaging device(s) in a direction transversely to a longitudinal axis of the imaging device(s) for accumulating a complete image over an imaging area.

In accordance with another aspect of the invention, there is provided a method of operating an imaging system with a slit- or slot-shaped imaging device as defined above, the method comprising moving the slit or slot shaped imaging device(s) in the transverse direction and reading accumulated charge from the pixel circuits of the slit- or slot-shaped imaging device(s) at a rate corresponding to movement of the imaging device(s) by half or less than half of the pixel size in the direction of motion.

In accordance with another aspect of the invention, there is provided a method of operating an imaging system comprising one or more slit- or slot-shaped imaging devices as defined above, the method comprising minimising the effect of scattered radiation by optimising the relationship between the following parameters: the distance between a radiation source and an object to be imaged; the distance between the object to be imaged and the slit- or slot-shaped imaging device(s); and the width of the slit- or slot-shaped imaging device(s).

The invention also provides a method for imaging accumulated values corresponding to respective pixel positions within a pixel array, such as, for example, charge values accumulated for respective pixel positions of an imaging device as defined above, the method comprising:

- determining maximum and minimum accumulated values for pixels within an area of the pixel array to be imaged;

- assigning grey scale or colour values at extremes of a grey or colour scale to be imaged to the maximum and minimum accumulated values; and

- assigning grey scale or colour values to the accumulated values for individual pixels scaled in accordance with the extreme values; and

- imaging the assigned grey scale or colour values at respective image pixel positions.

In other words, for each portion of an image captured by an imaging device in accordance with the invention, the charge density of all pixels to be displayed is compared, the points of highest and lowest charge density being assigned a colour value at the two extremes of the grey or colour scale being used. The remainder of the pixels points are given a value from the grey or colour scale according to the charge accumulated in the respective pixels.

The invention also provides a method of automatically optimising imaging using, for example, an imaging system as defined above for different imaging applications where incident radiation leaves a different electrical signal in a pixel detector of a semiconductor substrate dependent on a semiconductor material or compound used and an energy and a type of incident radiation, the method comprising:

- determining an expected best resolution using a centre of gravity technique;

- determining an expected efficiency as a function of radiation type and energy; and

- determining a pixel size and thickness as a function of a selected radiation type and energy and a selected semiconductor material or compound.

This method can also include a step of automatically selecting an imaging device having the determined pixel size and thickness.

This method enables automatic optimisation of the image

processing for different imaging applications where, dependent on the semiconductor material or compound used, incident radiation leaves a different electrical signal related to the energy and type of the incident radiation. In accordance with this method, the expected best resolution is identified using a centre of gravity technique. Similarly an expected efficiency is determined as a function of radiation type and energy. For each ASID semiconductor material or compound a database provides values for the various radiation types and energies, thus allowing an immediate and automatic optimization of design specifications. For example if silicon is to be used and the application is mammography at 15keV-40keV with required efficiency 30% the database can determine automatically the pixel size and thickness.

The invention also provides a method for automatically detecting and eliminating detected pixel value representative of radiation incident on a pixel cell of an imaging device, for example an imaging device as defined above, the method comprising:

- comparing the detected pixel value to a threshold value related to a minimum detected charge value expected for directly incident radiation; and
- discarding detected pixel values less than the threshold value.

Thus this aspect of the invention enables incident radiation (in particular low intensity radiation) that has been scattered before entering the imaging device to be eliminated before processing. This is done by discriminating the detected radiation according to the energy deposited in the form of electrical signals. Because scattered radiation has lost some of its energy it will not pass the minimum energy cut-off.

Another aspect of the invention also provides a method for performing real time imaging of an organic or inorganic object, the method comprising:

- irradiating the object using a radiation source that produces X-rays, γ-rays, β-rays or α-rays;
- detecting at a semiconductor imaging plane or planes of an imaging device as defined above unabsorbed radiation or radiation that is emitted from selected areas of the object, whereby charge resulting from incident radiation at respective pixel cells of the imaging device is accumulated in respective active circuits of the pixel cells;

- addressing the active circuits of the pixel cell individually for reading out accumulated charge;
- processing the read out charge to provide image pixel data; and
- displaying the image pixel data.

Thus, in addition to providing a new imaging device, the invention also provides systems utilizing the imaging device. In a first preferred configuration the imaging pixels are arranging in an M X N matrix where M and N can be several thousands thus providing a full field imaging plane. In another preferred configuration the imaging pixels are arranged in a slit or slot shape with several thousand rows and a few columns per row. The slit or slot is moved at a constant speed over a surface to be imaged and the slit (or slot) frame is read out fast enough so that the distance scanned between adjacent frames is smaller than half the pixel size along the direction of motion. With this configuration and mode of operation it is possible to achieve a point resolution along the direction of motion which is equal to the pixel size in the same direction. Thus, it is possible to improve by a factor of 2 the position resolution obtained with a full field imaging plane or a conventional slit or slot not operating in the mode described. In another preferred arrangement several of the above slits (or slots) are arranged on the same plane parallel to each other and with a constant distance between the longitudinal axis of the slits (or slots). Thus, if there are n such slits (or slots) and the total distance to be scanned is X cm than each slit (or slot) only needs to scan X/n cm. This will reduce the need for high speed scanning mechanics, and the same image can be formed for a unit period of time with the X-ray source operating at a lower current (n times lower current that with a single slit/slot).

The invention also provides a method of operating an imaging device or imaging system as defined above comprising reading the accumulated charge from individual pixel circuits at a rate to optimise the resolution of an analogue to digital converter for converting analogue accumulated charge values into digital values.

The invention also provides methods to utilize the device and system as described.

Thus, the invention provides active accumulative analogue imaging of directly detected high energy rays (e.g. energies greater than

10keV) as opposed to conventional digital imaging techniques based on the counting of hits. According to the invention, a charge (or current or voltage equivalent) value is accumulated rather than a number of points, the charge value being in direct and linear correspondence with the total energy of the initial rays. This is significantly different from the operational mode of CCDs that need a converting screen which degrades the energy resolution and compromises between efficiency and position resolution. Also it is different from counting points which have been assigned a value of 1 after a threshold cut, this being a technique limited to low intensity regimes where single counting is possible.

In accordance with an aspect of the invention a method is provided for accumulating charge into an image with the highest contrast and resolution for a given portion of the image. For every portion of the image this can be done by comparing a charge density of all pixels. The point of highest and lowest charge density can be assigned a colour value of the two extremes of the grey or colour scale that is used. The rest of the points are given a value from the grey or colour scale according to the charge (or current or voltage equivalent) accumulated for those pixels.

The invention also provides a method for minimising the effect on image resolution of rays that have been scattered before entering the imaging device. Accordingly, when the mode of active, accumulative analogue imaging of directly detected rays is effective, the scattered rays will have a much smaller weight in the contrast scale since they will have deposited much less energy in the imaging device. The deposited energy corresponds to a charge value (or current or voltage equivalent) that, for unscattered rays, is much higher. Thus, when during image processing each pixel is assigned a colour or grey scale value according to the charge value accumulated, the effect of scattered radiation can be minimised.

The invention also provides a method for excluding rays that have been scattered, either coherently or incoherently, before entering the imaging device. A slot technique is used to this effect with a collimated ray source which is adjusted to emit rays which are aimed at an imaging slot. By optimising the distance separating the ray source from the object under observation, the distance separating the object

under observation from the imaging slot and the width of the slot a geometry can be determined which minimises the detection of scattered rays. This is a result of scattered rays "seeing" a small phase space and having "no reason" to enter the thin imaging slot. This method is particularly powerful as it is a geometric technique and does not require knowledge of the energy of the rays. Scattered rays, whether they have been scattered incoherently and have lost some of their energy (Compton scattering) or coherently and have preserved all their energy (Rayleigh scattering) will most likely not be detected.

The invention also provides for excluding from detection radiation which has been scattered before entering the imaging device in low intensity applications. Through the use of a threshold to eliminate detected radiation with an energy below a predetermined value, energy which has been scattered incoherently and has lost some of its initial energy can be eliminated from detection.

The invention also enables the automatic optimisation of a particular configuration for each imaging application. A different electrical signal will be deposited in dependence upon the semiconductor material used and the type and energy of the radiation. An expected best resolution can be found using a centre of gravity method. An expected efficiency is a function of radiation type and energy can also be determined. For every semiconductor pixel material or compound a data base can provide values for various radiation types and energies, thus allowing an immediate and automatic optimisation of the design specification. For example, if silicon is to be used and the application is mammography at 15keV - 40keV with a required efficiency of 30%, the data base can automatically determine a pixel size and thickness.

An imaging device or an imaging system as defined above can be used for conventional X-rays, for chest X-rays, for X-ray mammography, for X-ray tomography, for computerized tomography, for X-ray bone densiometry, for γ-ray nuclear radiography, for gamma cameras for single photon emission computerised tomography (SPECT), for positron emission tomography (PET), for X-ray dental imaging, for X-ray panoramic dental imaging, for β-ray imaging using isotopes for DNA, RNA and protein sequencing, hybridization in situ, hybridization of DNA, RNA and protein isolated or integrated and generally for β-ray imaging

and autoradiography using chromatography and polymerars chain reaction, for X-ray and γ-ray imaging in product quality control, for non-destructive testing and monitoring in realtime and online, and for security control systems.

Exemplary embodiments of the invention are described hereinafter by way of example only with reference to the accompanying drawings in which:

Figure 1 is a schematic block diagram of an imaging system including an embodiment of an imaging device in accordance with the invention;

Figure 2 is a schematic circuit diagram of one example of an pixel circuit for an imaging device in accordance with the invention;

Figure 3 is a schematic diagram of part of an imaging array and control electronics for an imaging device in accordance with the invention;

Figure 4 is a schematic circuit diagram of part of an imaging array and control electronics for an imaging device with blocks of pixel cells of an imaging device in accordance with the invention;

Figure 5 is a schematic diagram showing a plurality of imaging devices tiled to form a mosaic of imaging devices in accordance with the invention;

Figure 5A is a schematic diagram of part of the control electronics for an embodiment of the invention comprising a plurality of imaging devices tiled to form a mosaic;

Figures 6A-6C are schematic diagrams of an imaging device in the form of a tile;

Figures 7A-7D illustrate an example in which two imaging planes are located on opposite sides of an object to be imaged in accordance with one application of the invention;

Figure 8 is a schematic circuit diagram of another example of an pixel circuit for an imaging device in accordance with the invention;

Figure 9A and 9B are schematic block diagrams of parts of an imaging array and control connections, respectively, for the embodiment of Figure 8;

Figure 10 is a cross-section view of the substrate of an example of an imaging device in accordance with the invention;

Figure 11 is a schematic circuit diagram of another example of an

pixel circuit for an imaging device in accordance with the invention;

Figure 12 illustrates an imaging technique in accordance with the invention using a slit- or slot-shaped imaging device;

Figure 13 illustrates the optimisation of parameters for a slit- or slot-shaped imaging device to reduce the effects of scattering; and

Figure 14 is a schematic illustration of the passage of β-rays through silicon.

Figure 1 is a schematic representation of an example of an application for an imaging system 10 including an embodiment of an imaging device in accordance with the invention.

This application relates to radiation imaging of an object 12 subjected to radiation 14. The radiation may, for example, be X-ray radiation and the object 12 may, for example, be a part of a human body.

The imaging device comprises an Active-pixel Semiconductor Imaging Device (ASID) 16 comprising a plurality of pixel cells 18. The imaging device detects directly high energy incident radiation such as X-rays, γ-rays, β-rays or α-rays and accumulates at each pixel cell, by means of a randomly accessible, active, dynamic pixel circuit on or adjacent to a corresponding pixel cell detector, values representative of the radiation incident at that pixel cell.

An ASID is distinctly different from, for example, a CCD. CCDs do not enable the imaging of high energy radiation (e.g., in excess of 10keV) directly incident on the CCD device. Also, CCDs do not include active pixel circuits for charge accumulation.

The ASID can be configured as a single semiconductor substrate (e.g., silicon) with each pixel cell comprising a pixel detector 19 and an active pixel circuit 20. Alternatively, the ASID can be configured on two substrates, one with an array of pixel detectors 19 and one with an array of active pixel circuits 20, the substrates being mechanically connected to each other by, for example, conventional bump-bonding technology.

Each pixel cell 18 is in effect defined on the substrate by electrodes (not shown) which apply a biasing voltage to define a depletion zone (i.e., the pixel detector 19) for the pixel cell 18. Active pixel circuits 20 in the form of electronic structures (e.g., of transistors, capacitors, etc.) can be defined on each pixel cell 18 or

at a corresponding location on the associated second substrate to accumulate charge created in the pixel detector when, for example, a photon or a charged particle of radiation is incident on the depletion zone of the pixel cell 18. An active pixel circuit 20 and the pixel detector 19 can be of the order of a few tens of microns in size. Examples of active pixel circuits are described hereinafter with reference to Figures 2, 8 and 11.

As mentioned above the active pixel circuits 20 can be constructed integrally to the semiconductor substrate 16 on the pixel cells 18 as part of the semiconductor wafer fabrication process. Conventional wafer manufacturing techniques can be employed for fabricating the semiconductor wafer. Alternatively, the active pixel circuits 20 can be constructed on a second wafer and distributed to correspond to the pixel detectors 19 defined for respective pixel cells 18 on a first wafer. The wafers can then be connected together in a known manner using, for example, bump bonding so that the active pixel circuit 20 for each pixel cell 18 is located adjacent to (behind) and overlies the corresponding pixel detector 19 for that pixel cell 18.

The pixel detectors 19 are formed with a depletion zone such that, when a photon is photo-absorbed in the semiconductor substrate 16 at a pixel cell 18 creating an electric charge or when a charged radiation ionizes the depletion zone of the semiconductor substrate 16 at a pixel cell 18, an electric pulse flows from the semiconductor substrate depletion zone to the active pixel circuit 20 for that pixel cell 18. A value associated with the electric pulse is then accumulated in an active circuit element, either directly as a charge value or as an equivalent voltage or current value such that new charge created from subsequent incoming radiation is added continuously. Example of possible accumulating devices are an integrated capacitor or the base junction of an integrated transistor. The charge accumulation process in an active pixel circuit 20 continues until control signals are issued from control electronics 24 to start a process of reading out information by addressing each pixel cell, effectively in a random access manner, from each individual pixel cell. After readout of the accumulated value from a pixel cell has been completed, which can be achieved very rapidly, the pixel cell circuit is active again to accumulate new charge. As each pixel cell stores charge values in a

respective active circuit which can be addressed individually, the problem of ambiguous points experienced with the prior art can be avoided completely.

The pixel pitch can be as small as 10μm which results in excellent position resolution and consequently excellent image resolution.

Figure 2 illustrates one preferred example of an active pixel circuit 20 for a pixel cell in an example of an imaging device in accordance with the invention. This example of the invention uses field effect transistors (FETs) arranged as a cascode connected amplifier. VBIAS 40 is a bias voltage input across the depletion zone forming the pixel detector 19 of the pixel cell. The pixel detector 19 is represented by the diode symbol D11. In the pixel circuit itself, SIGOUT 42 is an analogue signal output and VANA 44 an analogue power supply input. RES-R-1 is a reset input and ENA-R-1 is an enable input for the pixel circuit. Charge is accumulated in the gate of a transistor M11A 50 when both the RES-R-1 46 and ENA-R-1 48 inputs are low. To read the pixel cell, ENA-R-1 is taken to a high state, which allows current to flow from the transistor M11A 50 through the transistor M11B 52 to SIGOUT 42. The pixel circuit is reset by taking RES-R-1 to high, whereupon after RES-R-1 has been at high for merely a few microseconds, any accumulated charge will have been removed from the gate of the transistor M11A 50. Immediately after RES-R-1 46 goes to a low level, charge can begin to accumulate at the gate of the transistor M11A 50. If no reset pulse is supplied to the reset input RES-R-1 46, then it is to be noted that a reading operation when the enable input ENA-R-1 goes high does not destroy the charge but instead merely causes a current flow directly proportional to the accumulated charge.

While CCDs suffer from low sensitivity, low storage capacity and are static devices and are not addressable, conventional pixel detectors are more sensitive with higher resolution and readout speeds that depend on the number of pixels but do not accumulate charge and still cannot be addressed on a one to one basis. An active pixel circuits such as the circuit illustrated in Figure 2 can form, in combination with a pixel detector, a randomly accessible active, dynamic pixel cell for an imaging device in accordance with the

invention.

A pixel circuit 19 can accumulate an electric charge representative of up to 60,000,000 electrons (86 times that of a CCD) on each pixel. The pixel thickness of portion of the pixel detector that is fully depleted can be up to 3mm, thus making these detectors very sensitive to X-rays with energies less than 200keV. For charged radiation the sensitivity is practically 100%. The minimum pixel thickness can be of the order of 200μm which can give improved resolution when lower energy charged radiation is to be detected. The dead layer of the semiconductor substrate which is insensitive to radiation can be as thin as 50nm so that a signal from β-radiation with energies less than 30keV is not lost.

Figure 3 is a schematic representation of one possible configuration of the control electronics 24 of Figure 1 and the relationship of the control electronics 24 to an m x n matrix of the active circuits 20 of the pixel cells 18. For ease of illustration an array of 9 pixel cells is illustrated in Figure 3 and only some of the signal lines which make up the path 22 in Figure 1 are shown. It will be appreciated that an imaging device in accordance with the invention will normally include a significantly larger number of pixel cells 18 than are shown in Figure 3. The row select logic 60 controls the row readout (ENA 74) and the row reset (RES 76) and the column logic 62 enables (COL-SEL) the readout of accumulated charge values from each pixel circuit 19 in response to a clock signal 79.

The control electronics 24 include row select logic circuits 60, column address logic circuits 62, power supply circuits 70, Analogue to Digital Converter (ADC) 56 and the signal processing circuits 58. Preferably some, if not all, of the control electronics 24 is implemented on the substrate 16 at the periphery of the image array formed by the array of pixel cells 18.

The power supply circuits 70 provide power for the individual active circuits 20 on the pixel cells 18 via lines 54 (shown schematically in Figure 3) and can additionally be arranged to supply the biasing voltage via lines (not shown) for the electrodes defining the pixel cells.

The row select logic 60 provides signals via row enable and reset lines 64 and 66, respectively (also shown schematically in Figure 3),

for selecting columns for the reading and resetting, respectively of the individual active circuits 20 of the pixel cells 18. The row select 64 and row reset 66 lines are connected to the enable input ENA-R-1 48 and the reset input RES-R-1 46, respectively of each of the pixel circuits of the row. Also shown in the row select logic 60 are row enable 74 and row reset 76 signals for scanning successive rows. It can be seen that the reset pulse 76 follows the row enable pulse 74 to cause resetting of the active circuits after reading.

The column select logic 62 effectively comprises a multiplexer for selecting signals output via the column lines 68 (also shown schematically in Figure 3), each column line being connected to the SIGOUT output 42 of each pixel circuit 20 in that column. The COL-SEL signal 78 represented in the column select logic 62 thus selects columns for reading the individual active circuits 20 of the pixel cells 18 currently selected by the row enable pulses 74. In the embodiment shown the column select pulse is clocked for successive column positions in response to the clock CLK 79 during one row enable period, so that the accumulated charge value of a respective active pixel circuit on the row currently selected is clocked out at each clock pulse before the row select pulse proceeds to the next row. Each active pixel circuit of the row just read is then reset simultaneously by the row reset pulse 76.

The connections shown in Figure 3 are readily realisable using conventional double metallisation technology. Although, as described with reference to Figure 3, the pixels are read out sequentially in a predetermined order, it will be appreciated that the pixels are in effect accessed in a random access manner by means of separate row and column enable signals. It will be appreciated also that the scanning direction could be reversed (rows to columns) or indeed individual pixels could be accessed in a totally random order by suitable row and column enable signals. It will also be appreciated that the degree of sequential or parallel processing can easily be modified to match the needs of each application. For example all rows can be set simultaneously at an enable high state so that the column select clock will output in parallel all rows, thereby increasing the readout rate. The resetting of rows need not match the readout rate. After multiple readings each row may be reset at a lower rate than the readout rate.

It will be appreciated that the designation of rows and columns is arbitrary and can be reversed.

To cover a very large imaging surface in an effective way, the pixel cells are preferably grouped in blocks of m x n pixels with the pixels within a block being read out and reset sequentially in rows. Figure 4 is a schematic diagram showing a block of two rows by four columns of pixel circuits 20. The pixel circuits accumulate charge on the gates of the transistors MijA, where i=1,2 and j=1,2,3,4. In order to keep the transistors at a low potential, each gate is grounded after reading. Readout is initiated by applying a clock-pulse train to the CLK input 80, and a one clock period high (read bit) to an RB-IN input 82.

During the first clock period the RB-IN input 82 enables the switch SW4, which connects the analogue output line 68 for the fourth column to the analogue output ROUT 88. Thus, when the row enable input ENA-R-1 for the first row is high, which opens the switch transistors M1*B 52 of the first row, during this first clock period, a signal current representative of any charge stored on the gate of the transistor M14A 50 of the pixel circuit 20(1,4) flows through that transistor and via the switch SW4 to the analogue output ROUT 90.

By the next clock period of the clock CLK, the RB-IN input must be down. The high state, originally at the input of a flip-flop U1 is clocked by the clock train CLK to the input of a flip-flop U2 and switch SW3 which then connects the analogue output line 68 for the third column to the analogue output ROUT 88 so that a signal current representative of any charge stored on the gate of the transistor M13A 50 of the pixel circuit 20(1,3) can flow through that transistor and via the switch SW3 to the analogue output ROUT 90. Because the SW4 is now low (down) the analogue output line 68 for the fourth column is disconnected. The read bit thus ripples through the switches SW4-SW1 and flip-flops U1-U4 for successive clock pulses of the clock CLK. The column enable flip flops U1-U4 form a first shift register.

When the read bit is clocked out of the flip-flop U4 it is clocked back to the flip-flop U1. It is also clocked to the clock inputs of row-enable logic U5-U7 and row reset logic U9-U11. Each time these receive a clock input from the output of flip-flop U4 they advance a read bit and a reset bit, respectively, the reset bit moving

one step behind the read bit. The row enable logic flip flops U5-U7 form a second shift register and the row reset flip flops U9-U11 a third shift register.

In this way, each time a row is read out, the read bit is moved up one row. Similarly the reset bit is moved up one row, but one row behind the read bit. When the reset bit is read out of the last flip-flop U11, it is supplied to the Read bit out RBO output 84 and a new read cycle can be initiated. The time between successive read operations should be sufficiently short to keep the gates of the transistors MijA at a relatively low potential, preferably below 1V.

The storage capacity of the transistors MijA depends upon the capacitance and the voltage on the gate of the transistor. The transistors MijA can withstand up to 10V, but it is desirable to keep the gate voltage well below this at up to about 1V. The gate capacitance can be up to about 10pF. This means that $6x10^7$ electrons can be stored. This is about 86 times the capacity of a CCD which stores charge within the storage well within the substrate.

In practice the blocks will contain many more than 2 x 4 pixels. In an exemplary embodiment of the invention for use in mammography, each block includes 80 x 240 pixels. Mammography is perhaps an application for the present imaging device with some of the most stringent requirements with regard to readout speed and storing capacity. A successful mammographer should be able to record 10^4 X-rays at 20keV in one second for each pixel. Where each pixel circuit has a storage capacity of $6x10^7$ electrons, this means that more than ten thousand (10^4) X-rays can be accumulated on a pixel before the content of the pixel needs to be read out. It follows therefore that each pixel can for example be read of the order of 10 times per second or less, which equates to a pixel read out rate of 10Hz. In a block with 80 rows of 240 pixels each, the readout time of the whole block is defined by the clock rate divided by 19200, which is the total number of pixels in the block. For a clock rate of 10MHz, which is a typical clock rate, the whole block can be read at a rate of 520Hz. As only 10Hz is needed for mammography, it can be seen that the present embodiment of the invention is capable of handling intensities of up to fifty times that required for mammography.

One aspect to the operation of the device is the dead time, which can be defined as the time it takes to reset each row after it has been read out. A row of pixels can be reset in 10μsec, or less. During this time the pixels are inactive. Since in one second (which is typical for a mammogram) ten or less readout and reset operations are to be performed, this means that the total dead time is 0.0001 sec, or 0.01% dead time compared to the total time for which the imaging device needs to be active. The dead time with the present embodiment of the invention is insignificant therefore, and as good as no dead time. In order to appreciate how small this dead time is it is noted that the number of X-rays lost during this time (assuming 10^4 X-rays per pixels per second) is 10^4 x 0.0001 (approximately 1 X-ray per pixel). This is very much smaller than the quantum fluctuation limit (100) which is the statistical error for ten thousand X-rays. Accordingly this embodiment of the invention operates with a performance which matches the maximum possible statistically obtainable performance.

The example of a pixel circuit illustrated in Figure 2 can be implemented with major dimensions less than 35μm, so that the pixel cells may be 35μm square or less. Each block thus has dimensions of 4mm x 12mm and imaging surface for mammography having a surface area of 18cm x 24cm can be formed from a mosaic of a few hundred tiles, where each tile corresponds to a block of, for example, 115 x 341 pixel cells.

Using a tiling approach for the generation of large imaging surfaces has the advantage of high manufacturing yield. It also provides the advantage of modularity so that if one tile fails, it is possible to replace the tile without having to replace the whole imaging surface. This makes a large imaging array economically viable.

Surprisingly, it is still possible to obtain good imaging quality using a tiling approach, despite the tiles comprising the blocks of m x n pixels cells and the associated circuitry and control electronics. Each tile will need a minimum of four, possibly five to ten external contacts. Also, on each tile at the edge of the active image area comprising the array of m x n pixel cells, there is some inactive space where the control and logic circuits of the tile are placed. In a preferred embodiment of the invention, the tiles are therefore placed

in a mosaic as illustrated in Figure 5.

For use in mammography, a detecting plane should be of the order of $30x30cm^2$. No dead space is allowed in the detecting plane. To achieve this with the arrangement shown in Figure 5, the mosaic moves in two steps so that the whole surface to be imaged can be completely covered by accumulating three image frames. The tile shape can be substantially rectangular. The optimum length of the detecting (or active) area of one tile is equal to two times the total dead space at the long sides. As, however, estimated tile alignment accuracy of 50-100μm demands some overlapping of the active area of the tiles, the tile dimensions may not correspond to the optimum dimensions. An example of the possible mosaic for a mammography application can comprises 621 tiles, with each tile having 41760 pixel cells each of $35x35\mu m^2$.

The movement of the image mosaic can be achieved using conventional mechanical arrangements with sufficient accuracy and speed. Figure 5 illustrates that sufficient space has been provided for the electronics on each tile. The arrangement illustrated in Figure 5 is optimised to allow a full surface image to be produced with the three images being collected, respectively before, between and after two steps of 12mm. However, it will be appreciated that other embodiments may employ variations from the layout shown in Figure 5.

Figure 5A illustrates a part of the control electronics for an embodiment of the invention comprising a mosaic of tiles, for exampl as shown in Figure 5.

The basic control electronics for each tile (e.g. T2) corresponds generally to that shown in Figure 3. However, rather than one ADC 56 being provided for each tile (as shown in Figure 3), the outputs from a plurality of tiles (e.g. T1 - T10) are connected via a master multiplexer MM (e.g., operating at a 10MHz clock rate) to a common ADC 561 and from there to the signal processing logic, display etc. 58. The master multiplexer MM does not need to be placed on the tiles themselves, but can be located proximate thereto. The ADCs 561 are also not provided on the tiles but are preferably located nearby.

An advantage of the use of a master multiplexer is that the number of ADCs needed can be reduced, thus reducing the overall cost of

the imaging system. The high resolution ADCs form an expensive part of the overall system, so that reducing their number can have a significant effect on the overall cost. In an application such as mammography which can include a mosaic of several hundred tiles, a minimum of about nine ADCs are needed (i.e., just nine output channels) in order to provide the desired readout performance, even for high intensity mammography applications. The circuitry in accordance with the invention enables tiles to be read out in a controlled manner such that an image can be accumulated by reading out the tiles a plurality of times. This is something that cannot be done with, for example, a CCD device. The multiple reading of the tiles enables a contrast improvement in the following manner. As an example consider that 5000 X-rays are incident on a detector pixel. If the storage capacity of the pixel can handle all 5000 X-rays, it might be decided to set the readout rate to correspond to a timing for the receipt of 5000 X-rays so that analogue charge values for all 5000 X-rays can be stored at a pixel and then the total accumulated charge value is read out. If a 10-bit ADC (i.e. 1024 grey scales) is used every 4.88 X-rays (i.e. 5000 X-rays/1024) will then corresponds to a different grey scale quantisation. However, if a faster readout rate is used, for example at a timing corresponding to the reception of 1000 X-rays and the same ADC is used, then every 1000 X-ray/1024 = 0.97 corresponds to the grey scale quantisation. From this schematic example, it can be seen that the grey scale resolution can be increased by simply reading out at a higher rate.

The techniques described immediately above and with reference to Figure 5A enable an optimisation between cost (more multiplexing and less ADCs) and image contrast (less multiplexing and more ADCs).

Figures 6A-6C illustrate in more detail the construction of one example of a tile having a layered construction including a hybrid supporting board 210, a silicon readout chip 212 mounted on the supporting board and a pixel detector layer 214 made of, for example, CdZnTe, CdTe, HgI_2, GaAs, Ge, Si or TlBr and bump bonded to the readout chip. Figure 6A is a plan view of the pixel detector layer 214, which in this example has an active surface area 216 of 19.985mm x 19.985mm. Around the active surface area of the pixel detector layer is an inactive area including a detector guard ring 218. Figure 6B is a plan

view of the detector layer mounted on the readout chip 212 and the supporting board 210. It will be appreciated that as well as the detector guard ring 218, the inactive area surrounding the active detector area also includes the edges of the readout chip 212 and the hybrid supporting layer 210 and space needed between the tiles. Wire bond pads 220 on the supporting layer or board 210 permit the electrical connection of the readout chip to circuitry on the board 210 and from there via a master back plane to image processing circuitry. Figure 6C is a transverse cross-section of the tile showing the detector layer 214 connected at individual pixel locations to the readout chip by bump bonding 222. The supporting board is provided with an array of pins 224 for positioning and connecting the tile on a master back plane.

Figures 7A-7D illustrate an alternative to the provision of translation of a single detecting plane described with reference to Figure 5, for example for an application in autoradiography where the surface to be imaged emits radiation rather than an external source. Consider an example of autoradiography where a sample is labelled with isotopes (e.g., C14, P32, P35, S32, I125, H3, etc). and is positioned as close as possible to an image detector (for example an imaging plane as illustrated in a Figure 7A. Usually the sample rests on a thin mylar layer about 1.5 μm thick to avoid contamination. If the sample is located on the imaging plane, motion of the imaging plane as described with respect to Figure 5 would not be possible. However, as a result of the inactive areas around the active areas of the tiles, the active imaging area of a single mosaic layer as in Figure 7A will only provide about 85% coverage of the total area. Figure 7A illustrates some of the dimensions for one example of a tile mosaic.

A solution to this problem as illustrated schematically in Figures 7B and 7C is to provide a sandwich of two imaging planes DP1 and DP2, above and below, respectively, the sample OS. The second imaging plane is brought as close as possible to the first imaging plane with the sample in between, with the imaging planes parallel to one another and slightly displaced with respect to one another. The positional accuracy can be as good as 1-2μm. Figure 7D represents the dead or inactive space between the active imaging areas in the arrangement shown in Figures 7B and 7C. The white spots represent the

inactive areas with the cross hatched areas showing where the active areas overlap and the remaining hatched areas showing where only one active area overlies an area of the sample. In the particular example shown, and as identified in Figure 7D, only 1.2% of the total area is inactive, 68.9% is imaged by both imaging planes (thus increasing efficiency as radiation is detected on both sides of the sample) and 29.9% imaged by only one plane. The 1.2% of inactive area can still be covered by occasionally lifting the upper plane and displacing it slightly along the diagonal, for example.

Ideally, in autoradiography, image surfaces as large as 42cm x 39cm are needed. With tile dimensions as mentioned above, and 35μm x 35μm pixels, 98.8% of the total area can be covered with 578 tiles. Only 40 ADCs or less would be needed if the tiles are multiplexed together as described elsewhere herein. Using these techniques a new total image could be generated and displayed every 3 seconds. This application of the invention can give practically 4 π coverage of a sample increasing overall efficiency, real time imaging, a spatial resolution of 35μm and a dynamic range of 6 orders of magnitude.

Thus this alternative arrangement is suitable for use in applications where the object to be imaged includes a source of radiation is to provide first and second detecting planes arranged substantially parallel to one another and spaced from one another with an object source to be imaged between the detecting planes. By arranging for the tiles of the respective imaging planes to be offset laterally with respect to one another, it is possible to obtain substantially complete imaging of an object where the radiation from the object is substantially the same towards both planes.

Other configurations of imaging devices can be used in different applications. For example, for computerized tomography applications, the imaging devices are arranged substantially tangentially around the periphery of a ring or part-ring to encircle or partially encircle a slice of an object to be imaged. The imaging devices could also be arranged substantially tangentially around the periphery of a plurality of rings or part-rings displaced from one another in the direction forming a common axis of said rings or part-rings in order to image a plurality of slices of the object. In other applications the imaging devices could be tiled together to form a mosaic matching the area and

shape of an object to be imaged and/or to form a mosaic surrounding part or all of an object to be imaged.

Returning to Figure 1, the control electronics 24 include the processing and control circuitry described with reference to Figures 3 and 4, which is connected to the pixel cells 18 on the semiconductor substrate as represented schematically by the two-way arrow 22. The control electronics 24 enable the active circuits 20 associated with individual pixel cells 18 to be addressed (e.g., scanned) for reading out charge accumulated in the active circuits 20 at the individual pixel cells 18. The charge read out is supplied to Analogue to Digital Converters (ADCs) for digitisation and Data Reduction Processors (DRPs) for processing the binary signal.

The processing which is performed by the DRPs can involve discriminating signals which do not satisfy certain conditions such as a minimum energy level. This is particularly useful when each readout signal corresponds to a single incident radiation event. If the energy corresponding to the measured signal is less than that to be expected for the radiation used, it can be concluded that the reduced charge value stored results from scattering effects. In such a case the measurement can be discarded with a resulting improvement in image resolution.

The control electronics 24 is further interfaced via a path represented schematically by the arrow 26 to an image processor 28. The image processor 28 includes data storage in which it stores the digital value representative of the charge read from each pixel cell along with the position of the pixel cell 18 concerned. For each pixel cell 18, each charge value read from the pixel cell is added to the charge value already stored for that pixel cell so that a charge value is accumulated. As a result, each image can be stored as a representation of a two-dimensional array of pixel values which can be stored, for example, in a database.

The image processor 28 can access the stored image data in the database to select a given image (all the array) or a part of the image (a sub-sample of the image array). The image processor 28 reads the values stored for the selected pixel positions and causes a representation of the data to be displayed on a display 32 via a path represented schematically by the arrow 30. The data can of course be

printed rather than, or in addition to being displayed and can be subjected to further processing operations. Background and noise can be subtracted as a constant from each pixel charge value.

The operation of the image processor 28 will be described in more detail below. However, before passing to examples of the operation of the image processor, examples of other forms of imaging devices in accordance with the invention will be described.

Figure 8 is a circuit diagram of a further example of an active circuit 120 for a pixel cell 18 in accordance with an embodiment of the invention.

The pixel detector 19 is represented by the diode symbol 182 connected to the voltage bias Vbias 180, this being applied via the electrode (not shown) defining the depletion volume or pixel detector 19 of the pixel cell 18.

Charge created by radiation incident on the depletion volume 19 of the pixel cell 18 is input to the base of a first, input transistor 184 (here a field effect transistor (FET) having a transconductance of, for example, 0.3mS and a drain source current value I_{DS} of 100μA and a capacitance of 0.1pF). The source and drain of the input FET 184, are connected between a first current source 186 (here a suitably configured FET, although this could be replaced by a resistor) and a ground line GND 174. The current source 186 is in turn connected to a positive supply line V+ 172.

The junction between the input FET 184 and the current source 186 is connected to one terminal of a second transistor 188 forming a common base bipolar amplifier controlled by the bias voltage applied to its base. The base of the second transistor 188 is connected to the bias voltage line V_Q 178. The remaining terminal of the second transistor is connected via a feedback capacitor Cf 190 (e.g., with a capacitance of 0.3pF) to the base of the input FET 184.

The junction between the second transistor 188 and the capacitor Cf 190 is also connected to a second current source (here a suitably configured FET, although this could be replaced by a resistor) to a negative supply line V- 176. Charge resulting from radiation incident on the depletion volume of the pixel cell can thus be accumulated at the capacitor Cf 190.

X and Y read lines, Xread 160 and Yread 164, are connected to read logic 198 (here a dual base FET) which in turn is connected between the negative supply line V- 176 and an output switch 196 (here a FET) whereby charge collected on the capacitor Cf 190 can be output via an output line 156 when a signal is supplied on the Xread and Yread lines 160 and 164 simultaneously. The X and Y reset lines, Xreset 162 and Yreset 168, are connected to discharge logic 100 (here a dual base FET) which in turn is connected between the negative supply line V- 176 and a discharge switch 192 (here a FET 192) for discharging and thereby resetting the capacitor Cf 190 when a signal is supplied on the Xreset and Yreset lines 162 and 168 simultaneously.

The circuit shown in Figure 8 forms a charge sensitive amplifier with charge storage capability in the feedback capacitor Cf 190 and with output and resetting circuitry. Depending on the charge storage time and radiation hardness requirements, the FETs can be implemented by an appropriate technology such as JFET or MOSFET. If the capacitor Cf 190 has a capacitance of 0.3pF, this corresponds to a storage capacity of about 1.8 million electrons. If the capacitor Cf 190 has a capacitance of 1pF, this corresponds to a storage capacity of about 6 million electrons. The maximum output clock frequency with a reset FET in the output line is 1-5MHz. This maximum output frequency reduces to about 100kHz without a reset FET in the output line.

The circuitry illustrated in Figure 8 could be implemented on, for example, a pixel cell having a size of approximately 150 x 150 microns. Depending on the circuit technology used, smaller pixel sizes are also envisaged. For example, the active circuit 20 could also be implemented for pixel cells having a size of the order of 50 x 50 microns. A total of 1200 x 1200 pixel cells could be implemented on a single semiconductor substrate 16, giving an imaging area of the semiconductor substrate of approximately 60mm by 60mm. Multiple such planes can be placed next to one another (or tiled) thus giving, for example, an imaging surface as large, or larger than 400mm x 400mm. Around the outside of the imaging area formed by the array of imaging cells some or all of the control electronics 24 may also be implemented as an integral part of the semiconductor substrate wafer 16.

Figure 9A is a schematic representation of the control electronics 24 in more detail and the relationship of the control

electronics 24 to active pixel circuits 20 of the type illustrated in Figure 8 on the substrate 16. For ease of illustration an array of 16 pixel cells is illustrated in Figure 9A and only some of the signal lines which make up the path 22 in Figure 1 are shown. It will be appreciated that an imaging device in accordance with the invention will normally include a significantly larger number of pixel cells 18 than are shown in Figure 9A.

The control electronics 24 include X address logic circuits 144, Y address logic circuits 146, power supply circuits 150 and signal processing circuits 148. Preferably some, if not all, of the control electronics 24 is implemented on the substrate on which the pixel circuits are implemented at the periphery of the array of pixel circuits. The power supply circuits 150 provide power for the individual pixel circuits 20 via lines 170 (shown schematically on Figure 9A) and can additionally be arranged to supply the biasing voltage via lines (not shown) for the electrodes defining the pixel cell detectors. The X and Y addressing logic 144 and 146 provide signals via row and column lines 152 and 154, respectively, (shown schematically in Figure 9) for controlling the reading and resetting of the individual pixel circuits 20. The signal processing circuitry 148 is connected to output lines 156 shown schematically in Figure 9A for the active circuits 20. In the embodiment of Figure 9A, one output line is provided for each row of pixel circuits 20 and is connected via an output amplifier 158 to the signal processing circuitry 148. However, it will be appreciated that as alternatives separate output lines could be provided for each column, or for groups of rows or columns or for groups of pixel cells/circuits as desired.

Figure 9B illustrates in more detail the signal lines which are provided between the control circuitry 24 and a pixel circuit 20 for a pixel cell 18 in accordance with this embodiment of the invention. The power supply lines 170 comprises a positive supply line V+ 72, a ground line GRD 174, a negative supply line V- 176 and an amplification power line Vq 178. The row lines 152 comprise an Xread line 160 and an Xreset line 162 and the column lines 154 comprise a Yread line 164 and an Yreset line 166. One output line is provided for each row in this embodiment as has already been explained.

The pixel circuit shown in Figure 8 along with the connections

shown in Figures 9A and 9B can be implemented integrally on one semiconductor substrate using conventional integrated circuit manufacturing techniques or on two superimposed semiconductor substrates with an array of pixel detectors on the first substrate and an array of pixel circuits on a second substrate mechanically attached to the first, for example by bump-bonding, with a one-to-one correspondence between pixel detectors and their corresponding pixel circuits.

Figure 10 is a very schematic cross-sectional view of the semiconductor substrate 16 of an example of an imaging device in accordance with the invention on a single substrate. It is assumed in Figure 10 that incident radiation IR will be incident in a downwards direction onto the upper surface of the substrate 16 as represented in Figure 10. Each pixel cell 18 is defined by an electrode to which is supplied a bias voltage at 180. The extent of the pixel cell 18 is represented schematically by the dotted lines. For each pixel cell, active circuit elements 20 are provided towards the rear (here the bottom) surface of the semiconductor substrate. The active circuits 20 are connected to one another by means of the paths 22. The circuitry is provided to the rear of the substrate in order that it does not reduce the degree of radiation which can be incident on the pixel detector 19 of the pixel cell 18. It will be appreciated the Figure 10 is merely a schematic representation on the semiconductor substrate and is not shown to scale.

Figure 11 illustrates a further example of an active pixel circuit 320 for a pixel cell in an example of an imaging device in accordance with the invention. This example is similar to the example of Figure 2. The pixel detector is represented at PD 319 of the pixel cell. In the pixel circuit itself, VBIAS 340 is a voltage bias, OUT 342 is an analogue signal output, RESET 346 is a reset input connected to a reset FET 347 and ENABLE 348 is an enable input connected to an enable FET 352 for the pixel circuit. Charge is accumulated in the gate of a charge storage FET 350 when both the RESET 346 and ENABLE 348 inputs are low. To read the pixel cell, ENABLE 348 is taken to a high state, which allows current to flow from the FET 350 through the FET 352 to OUT 342. The pixel circuit is reset by taking RESET to high, whereupon after RESET 346 has been at high for merely a few

microseconds, any accumulated charge will have been removed from the gate of the FET 350. Immediately after RESET 346 goes to a low level, charge can begin to accumulate at the gate of the FET 350. If no reset pulse is supplied to the reset input RESET 346, then it is to be noted that a reading operation when the enable input ENABLE goes high does not destroy the charge but instead merely causes a current flow directly proportional to the accumulated charge. It will therefore be seen that the operation of the circuit of Figure 11 is similar to that of Figure 2. In addition, the circuit of Figure 11 includes diodes 354 and 356 which act as overload protection circuitry for the pixel circuit. The diodes provide protection both against static electricity which might damage the FETs and against FET overload. If the FET gate 350 accumulates more than a predetermined charge threshold (e.g., corresponding to 5 volts, which is the voltage bias) then current will start to flow through the diode 354 towards the VBIAS 340 thus protecting the FET 350. This will protect pixel cells which, for example, receive a full radiation dose outside the perimeter of an object to the imaged.

Rather than arranging pixel cells in a largely rectangular array, in other embodiments of the invention, the imaging device could be configured as a slit with pixel cells arranged in a single column or a slot with pixel cells being arranged in a number of columns side by side. A slit or slot can be used in many applications such as radiographic body scanning, dental panoramic imaging, security scanning, etc. The use of a slot can also be used as an alternative to full field scanning with the advantage of lower cost because of the lower imaging surface. In the case of a slit or a slot having one or two rows of pixels the pixel circuits could be located to the side of the corresponding pixel detectors on the same semiconductor substrate rather than behind the pixel detectors on the same or a different semiconductor substrate. A very long uninterrupted slit (or slot) could be formed by placing a number of slit (or slot) tiles end to end. By locating the control electronics to the side of the pixel cells formed by the pixel detectors and the pixel circuits, the pixel cells can extend substantially right to the end of the individual slit (or slot) tiles. In this way a very long uninterrupted slit (or slot) can be manufactured in a very cost effective manner.

Figure 12 illustrates an imaging technique in accordance with the invention using an imaging device in accordance with the invention with a slit or slot of random accessible, active dynamic pixel cells. In accordance with this technique, the slit or slot is moved sideways at a constant speed v and is read out every $t_1 - t_0$ time units.

In the example shown in Figure 12, a slit with 6 pixels, each pixel having the dimensions (x,y). The constant movement is in the direction of the dimension x. If readout occurs at time t_0, then in accordance with this aspect of the invention, the slit should be allowed to move until a time t_1 and then be read out again. The distance moved, or scanned, during the period $t_1 - t_0$ is dx and should not be larger than half the pixel size in the direction of movement (i.e. dx <= x/2). This technique improves the resolution along the axis of movement by a factor of two compared to full field imaging or conventional slit (slot) techniques. The reason for the improvement lies in the multiple sampling mode that is used and according to which if the slit (slot) frame is accumulated in short enough intervals (distance scanned must be shorter than half the pixel size), the underlying structure is 'sensed' with a resolution equal to the pixel size rather than twice the pixel size. Twice the pixel size is the effective resolution for a full field imaging plane or a slit (slot) that does not operate in the manner in accordance with this aspect of the invention. The above described technique can be used for example in dental panoramic imaging. The scan speed is typically 4cm/sec and the slot has a width of 4mm and a length of 8cm. This translates to 80 x 1600 pixels with a 50μm square pixel size. The whole image accumulation should last about 10 seconds. According to the current embodiment of the invention, the slot should be read out at least every 25 μm which means a slot readout rate of 1.6kHz. If blocks of pixels of 80 columns by 20 rows of pixels and a clock frequency of 5MHz are used, the block readout speed is $5 \times 10^6/(20 \times 80) = 3.1$kHz; much more than the 1.kHz needed.

When the slit (slot) technique is used the X-ray source should be set at a higher operating current or if possible the X-rays should be condensed from a full field area to the dimensions of th slit (slot). This is needed to keep the image accumulation time constant. In many

cases this can be technically difficult and costly. An alternative to the single slit (slot) technique is a multi-slit (-slot) technique. In accordance with this variant multiple slits (slots) are positioned on a plane parallel to each other and with some constant distance between the longitudinal axis of the slits (slots). In this manner, if there are n slits (slots) and the total distance to be scanned is X cm, then each slit (slot) need only scan X/n cm. This makes less demands on the mechanics, but more importantly the X-ray source energy needs to increase by only X/(n x slit (slot) width).

Various methods of operation of the imaging devices and systems in accordance with the invention will now be described. As mentioned above the devices and systems of the invention are aimed to proved imaging of high energy radiation which is intended to be incident directly on the imaging devices. In embodiments of the invention, charge is accumulated (by storing charge values directly or voltage or current equivalents) in response to radiation hits with the charge value being directly and linearly related to the total energy of the incident radiation, rather than by counting numbers of points or events. This is different from the approach which has to be adopted for a CCD, which requires a converting screen to convert high energy radiation to optical or ultra-violet wavelength, thus destroying the energy and position resolution. It is also different from simple pixels with buffer circuits that limit the operation to one of counting points after the application of a threshold cut and in the low intensity regime where single counting is possible.

As mentioned above with reference to Figure 1, after the ADCs, there is an image processor 28 which stores the digital value representative of the charge read from each pixel cell along with the position of the pixel cell 18 concerned. For each pixel cell 18, each charge value read from the pixel cell is added to the charge value already stored for that pixel cell so that a charge value is accumulated. As a result, each image can be stored as a representation of a two-dimensional array of pixel values.

The image data can be stored, for example, in a database as a two-dimensional array for the image:

Image $(1{:}N_{pixels}, 1{:}3)$

where the first index includes N_{pixels} items representing a pixel number on the imaging plane which runs linearly from one to a maximum pixel number N_{pixels} and the second index includes three values, for the x and y coordinates and the charge value accumulated for each pixel, respectively.

The image processor 28 access the stored image data in the database to select a given image (all the array) or a part of the image (a sub-sample of the image array) and causes a representation of the data to be displayed, printed, or processed further.

Preferably, before displaying, printing or further processing the image data, the image processor 28 finds the two extreme pixel charge values stored for the pixels selected and assigns these values to the two extremes of the grey or colour scale which can be used for displaying, printing or further processing of the image, as appropriate. The remaining charge values for the pixel positions can then be assigned an intermediate grey scale or colour value between these extreme values according to the charge deposited on the pixel. For example the grey scale value can be assigned to the charge values for individual pixels in accordance with the following equation:

$$\text{Grey scale value of pixel } i = \text{Min}_{grey} + \frac{(i_{charge} - \text{Min}_{charge})}{(\text{Max}_{charge} - \text{Min}_{charge})} \times (\text{Max}_{grey} - \text{Min}_{grey})$$

The selection of a portion of the image to be zoomed can be achieved by means of conventional user input devices 36 via a data path represented schematically by the arrow 34, possibly interacting with the display 32 as represented schematically by the double arrow 38. The user input devices 36 can include, for example a keyboard, a mouse, etc.

The invention brings a number of advantages as a result of accumulating charge in an active circuit for each pixel cell.

The ability to accumulate the charge in the active circuits on the pixel cells and then selectively to read out the stored charge from individually addressable active circuits in one to one correspondence with the pixel cells completely resolves any ambiguities regarding the point of incidence of concurrently incident radiation.

As the charge can be built up over a period on individual active

circuits, the readout speed need not be excessively high, with the result that, for example, software-based generation and processing of the image in real time is possible and indeed can be implemented inexpensively on readily available computer hardware.

For each portion of the captured image the contrast and resolution can be adjusted automatically and displayed on a full screen. Wherever there is a charge density variation between the pixel cells of an area of the image captured by the imaging device, features of the image can be resolved when that part of the captured image is displayed.

The dynamic range is effectively unlimited assuming that the charge from the charge storage device of the pixel cell active circuits is read and the charge storage device is reset repeatedly before the storage capacity of the charge storage device is exhausted. It is merely necessary to select the "refresh rate" of the active circuits, that is the frequency of reading out and resetting those circuits, to suit the storage capacity of the charge storage devices and the anticipated maximum radiation density. Thus, as more radiation creates more charge, this is stored in the active circuits of the pixel cells, then read out at appropriate intervals and digitized by the control electronics. After digitization, the charge has a known value that can be accumulated with existing digitized charge values of the same pixel. The only practical limitation is the maximum digital value which can be stored by the processing circuitry. However, even then the processing circuity could be arranged to detect a value approaching the maximum possible value which can be stored and then to apply a scaling factor to the stored values of all pixel cells.

The invention enables real-time imaging. Once an image array has been created, even before irradiation starts, the image array can be updated continuously with new digitized charge values from the imaging device, which charge values are then added to the existing charge values of the respective pixel of the array and the accumulated charge values are displayed in real time.

Where a continuously updated image array is employed, this provides an efficient use of computer storage as detected radiation will not yield more image points, as is the case with some prior techniques, but instead yields higher charge values for the pixel cell

positions concerned. In other words, the present invention enables the accumulation of radiation counts rather then generation of an ever increasing number of radiation hit points.

Thus, whereas CCDs suffer from relatively low intensity, low storage capacity and low charge resolution when used in conjunction with conversion screens and are static devices, and conventional semiconductor pixel detectors are more sensitive with high resolution but require high readout speeds and do not store charge, an imaging device of the ASID type in accordance with the invention can provide the advantages of conventional semiconductor devices with the additional advantages of enabling charge storage at the pixel cell level with random access readout at a lower rate.

The present invention offers a way to minimise the effect of radiation scattered before entering the imaging device. When an imaging device is used in the manner described above, scattered rays will lead to a lower charge value being accumulated than would be the case if that radiation was directly incident. This is because the scattered rays will deposit less energy in the depletion zone of the pixel detector. Thus, when processing the accumulated charge, scattered radiation will have a much lower effect on the overall accumulated charge than direct radiation. By assigning an appropriate grey scale or colour value to lower values when displaying an accumulated image, it is possible to minimise the effect of the scattered radiation.

For applications with radiation intensities requiring less than the maximum achievable readout speed per pixel (kHz range), the present invention offers a way of excluding the effect of radiation scattered before entering the imaging device, which, if not excluded, will degrade the image resolution. The way that this can be done will now be explained. The charge created from each and every photon or charged radiation particle is first stored in the active circuits of the pixel cells and then read out. The control electronics digitises the charge and the DRP can compare the digitized value to a threshold reference value. The reference value corresponds to the charge to be expected from incident radiation of the type in question, that is for example an X-ray of a given wavelength or from a charged radiation of a given energy. The digitised charge value is then excluded from further

consideration if it is less than the reference value. This discrimination operation enables scattered rays to be eliminated from consideration. When inelastic scattering effects occur before the imaging plane while, for example, the radiation traverses an object under observation, the scattered radiation loses some of its energy before the imaging plane so that less charge is created in the depletion region of a pixel cell. Such effects are Compton scattering for photons and ionization scattering for charged particles.

An example of a method which enables a way of excluding the effect of radiation scattered, either coherently or incoherently, before entering the imaging device using a slot technique and a collimated radiation source such that it is adjusted to emit rays that are aimed at the imaging slot. The distance between the ray source and the object under observation, the distance between the object and the imaging slot and the width of the slot are optimised. These parameters can be used to define the geometry that minimises detection of scattered rays. This is because the scattered rays 'see' a small phase space and have no reason to enter the thin imaging slot. This method is particularly powerful because it is based on geometry and does not require knowledge of the energy of the rays. If the rays have been scattered they will most likely miss detection whether they have been scattered incoherently and have lost some of their energy (Compton scattering) or coherently and have preserved all of their energy (Rayleigh scattering).

Figure 13 illustrates, by way of example, the ratio of unscattered radiation that reaches the slit (slot) as a function of the slit (slot) width for four different photon energies and four different distance between the slit (slot) and the object under observation. For this example, water is assumed to be the object that causes scattering with 10cm thickness. The semiconductor is assumed to be silicon. It is seen from the four curves that practically all scattering is excluded (100% vertical axis) at slot widths between 1mm and 4mm. This result is almost irrelevant to the distance between the slot and object (β in the Figure). If the slot width starts to be larger than 1 - 4mm, then the results starts depending on β as well. Thus, for a given energy and object under consideration, the optimal slot width and the distance β between the slot and the object is determined such that the

scattered rays will almost totally be excluded, thus dramatically improving the image resolution and contrast. This method enables the exclusion of coherently scattered rays, which could not otherwise be excluded as they have the same energy as the unscattered rays.

Imaging device design optimisation in accordance with the invention can be carried out in an predetermined automated manner. Each material or compound chosen for the semiconductor substrate has a different response to incident radiation which depends on the physical properties of the material or compound, the radiation type and the radiation energy. A centre of gravity method is applied to the deposited electric signal at every step as incident radiation traverses the semiconductor substrate. This enables the best attainable resolution to be determined as a function of the above parameters. Thus the pixel size is determined. By correctly choosing the pixel size the signal to noise ratio can be maximised (because most of the signal is contained in one pixel) while the cost and device complexity is minimized. These results along with the expected sensitivity can be stored in a database and can be used to define the design parameters of the imaging plane of the imaging device, namely the pixel size and substrate thickness. Alternatively, a series of imaging planes compatible with a common set of control electronics and image processor can be provided. An end user can then, before carrying out imaging, input a desired sensitivity to the image processor to cause this automatically to select an imaging plane with the correct specification.

Consider, as an example, the use of silicon as the semiconductor substrate material. In biotechnology applications, isotopes such as 3H, 35S, 32P, 33P, 14C and 125I are used. These isotopes emit β radiation. Consider 35S, for example, which emits 170keV charged radiation. Figure 14 shows the passage of many such β-rays through silicon. If the centre of gravity method is applied, it is found that the resolution cannot be better than 32μm. The pixel size can then be chosen to be greater than 32μm in order to contain most of the electrical signal. The β radiation isotopes mentioned above are used in most biotechnology applications. In mammography, tomography, nuclear medicine, dental imaging, security systems and product quality control X-rays are used with energies between 10keV-180keV and CdZnTe,

CdTe and HgI_2 are suitable choices of semiconductors.

By way of example if silicon is chosen as the semiconductor material, Table 1 illustrates design values for the image plane. Other semiconductors can be mapped in a similar way and stored in data bases, for example CdZnTe, CdTe, HgI_2, GaAs, Ge, Si, TlBr, etc. can be used in the embodiments of the invention.

	Pixel Size (μm)	Pixel Thickness (mm)
Isotopes (β-rays) 3H(18keV)	<10	0.2
14C(155keV)	27	0.2
35S(170keV)	32	0.2
33P(250keV)	58	0.2
32P(1700keV)	<10	0.2
α particles For energy>100keV	<10	0.2
Photons X-rays (10keV-30keV)	<10	0.3
X-rays (30keV-100keV)	<10	≥1.0
X-rays (>100keV)	50	≥1.0

Table 1: Design specifications as a function of radiation type and energy. These values enter a database and before execution of an application automatically determine the optimized imaging plane design.

There are many biology applications that perform imaging with β radiation. Most often one of the following isotopes are used: 3H(18keV), 14C(155keV),35S(170keV), 33P250keV), 32P(1700keV).

The precision requirements for these applications could be summarized as follows:

- hybridization in situ requires ideally 10μm;
- hybridization on DNA, RNA and protein isolated or integrated requires ideally better than 300μm;
- Sequences of DNA require ideally 100μm.

An imaging device in accordance with the invention can meet the above requirements. In addition the excellent efficiency (practically 100%) of imaging devices in accordance with the invention can reduce

the time for obtaining the results from days or months to hours. Since the imaging is done in real time a biologist can see the results while they are being accumulated. Software and statistical methods of analysis can be used for interpreting these results.

In mammography the X-rays used have typically energy from 10keV to 30keV. The X-ray source is placed behind the object under observation which absorbs part of the X-rays and lets the rest through. The X-rays that arrive at the imaging plane are consequently photo-absorbed and create an electrical signal from which the point of incidence is determined. The charge density distribution effectively defines the image, which, with on-line conventional processing can be coloured, zoomed and analyzed with maximum image contrast and resolution. With 0.5-1mm thick active CdZnTe, CdTe and HgI_2 pixels the efficiency is almost 100% and the dose needed can be reduced drastically. The resolution for mammography can be better than 30μm and organic structures of that size are revealed.

In nuclear medical diagnosis an isotope emitting X-rays at the range of 150keV (such as, for example, Tc^{99} with 6 hours half life) is injected to the human body and concentrates to certain areas that are imaged. The radiation is emitted isotropically and around the human body collimators filter away unwanted directions thus making projections of a point to different planes. According to an example of the current invention the ASID, made for example of CdZnTe, CdTe, HgI_2, GaAs, Ge or Si, can be placed in front of and around the human brain replacing existing imaging planes.

In dental operations imaging is performed with X-rays at energies of 40keV-100keV and imaging areas around 15 cm^2 to 25 cm^2 are needed. Dental panoramic imaging using the slit/slot technique described above thus forms a preferred application of the invention. Suitable semiconductors are as described above.

Yet another possible application of the invention is non-destructive industrial evaluation and product quality control. Depending on the inorganic object that is observed a different X-ray energy is chosen so as to optimize resolution with high contrast and efficiency. X-ray energies in the range 20keV-180keV may be used. The image of a product or a structure is automatically compared to an ideal

image of the same product or structure and various levels of severity may trigger different actions that give feedback to the production line.

Thus, there have been described a new device and method for imaging in applications that use any type of radiation (X-rays, γ-ray, β-rays and α-rays). An automated system for real time, high resolution, high efficiency and unlimited dynamic range imaging can be provided using the new active pixel semiconductor radiation detectors devices. The active pixels can be defined on a single semiconductor substrate or on a pair of linked substrates linked, for example, by bump bonding techniques, and charge is stored on circuit elements that are associated with respective pixel detectors. The pixels can be read out individually and all ambiguities that are present in a normal strip or CCD semiconductor detector are resolved. The imaging plane design can be predetermined depending on the radiation type, energy of radiation and object under observation. The stored charge on each pixel can be used to acquire an image with automatically adjusted high contrast and resolution. In one application the invention can be used in X-ray and γ-ray radiography with radiation energies from 10keV to 200keV. In another application the invention can be used for DNA, RNA and protein sequencing, in hybridization in situ and in hybridization on DNA, RNA and protein isolated or integrated. For this application the radiation isotopes are preferably (but not limited to) ^{3}H, ^{35}S, ^{33}P, ^{32}P, ^{14}C and ^{125}I. The invention can also be used for real time product quality control and security systems. It will be appreciated that the ASID described above, although intended specifically for use in imaging applications, is not limited to use in such applications. It could be used in other applications, for example as part of a radiation impact position detector, part of a radiation counter, etc.

Thus, there has been described a real time imaging system comprising:-

(a) An active semiconductor pixel imaging device (ASID) consisting of one or more semiconductor substrates with active circuit elements built thereon. The active circuit elements comprise integrated electronic structures such as capacitors and transistors which are able to accumulate the charge (or an equivalent voltage or current) created in the semiconductor substrate. The pixel size can be as small as 10μm

and the substrate thickness from 200μm to more than 3mm.

(b) Readout and control electronics that may or may not be attached to the semiconductor substrate, CPU and control modules, ADCs, discriminators and data reduction processors. These electronics control the readout and processing of the electric signals and are able to address each pixel individually (e.g., by scanning).

(c) An image processor interfaced to the second level electronics that converts the charge density to images.

(d) A workstation or PC that displays the images and carries out image analysis.

(e) A source of radiation located behind the organic or inorganic object under observation or injected in the form of isotopes to the object under observation and the isotopes consequently attach to selected areas that are imaged. The source of radiation can be X-ray tubes, synchrotron X-rays, ^{57}Co, ^{60}Co, ^{241}Am, ^{99}Tc, ^{3}H, ^{14}C, ^{35}S, ^{33}P, ^{32}P.

There has also been described a method for performing real time imaging comprising the following steps:-

(a) Select an organic or inorganic object to be observed.

(b) Select a radiation source that produces X-rays, γ-rays, β-rays or α-rays and placing the same behind the object under observation or injecting into the object and so that it becomes attached to selected areas.

(c) Arrange that the object under observation either absorbs partially the radiation that was incident upon it and lets through the rest or arranging that selected areas of the object to which the radiation source is attached emit radiation.

(d) Arrange that unabsorbed radiation or radiation that is emitted from selected areas of the object is detected at semiconductor imaging plane or planes that are positioned as close as possible to the object. The imaging plane(s) comprise active pixel semiconductor imaging devices (ASIDs) that convert directly incident photons or charged radiation to electrical signals stored on active dynamic electronic elements built onto pixel cells of the ASIDs.

(e) Individually address by means of control electronics each pixel to read out and consequently reset, if needed, the stored charge and process the same without ambiguities as to the point of incidence of

the radiation. The stored charge of each pixel is digitized to provide a value representative of the charge imparted to the pixel cell by the incident radiation.

(f) Interface the control electronics to an image processor that receives the information of the digitized charge value and stores it along with the pixel positions to an array. This is done for each pixel.

(g) Find in the image processor the maximum and minimum charge stored and automatically assigning grey or colour scale values to all selected pixels according to their charge and the minimum and maximum grey and colour scale values. This is done according to the formula:

$$\text{Grey scale value of pixel } i = \text{Min}_{grey} + \frac{(i_{charge} - \text{Min}_{charge})}{(\text{Max}_{charge} - \text{Min}_{charge})} \times (\text{Max}_{grey} - \text{Min}_{grey})$$

(h) Display each pixel position with a grey or colour scale value as shown above, on a computer screen.

(i) Continuously supply the image processor with new digitized charge values such that a previously stored image array is updated by adding the new charge values for a pixel to the existing value stored for that pixel and displaying the updated image on a display thus providing real time imaging.

(j) Store, at any given instant, the image array and retrieving the same later on to be analyzed, transferred to a different site etc. From a keyboard or using a "mouse" of the image processor, a user can select part of the image corresponding to part of the image array. The image processor the selects the corresponding pixels and displays them on the whole screen (zooming) while automatically adjusting the contrast and resolution according to step (g).

There has also been described a method for discriminating scattered radiation and improving imaging resolution comprising the following steps:-

(a) Receive and record the electrical signal of incoming radiation using an active pixel semiconductor imaging device.

(b) Process stored charge of every pixel including digitizing the same.

(c) Compare the digitized value of every pixel to a reference value

and if it is found to be smaller, the pixel value is reset and is not read out to an image processor.

There has also been described a method for automatic design optimization of the imaging plane parameters and automatic choice of the correct design at execution time comprising the following steps:-

(a) Provide a database with materials, compounds, radiation type, energy and desired sensitivity. For each of these items a value for the optimal size of the active semiconductor pixels and a value of the thickness of the active semiconductor pixels is provided.

(b) Use these parameters to determine the optimal design solution by maximizing signal to noise ratio and minimizing cost and complexity.

(c) Alternatively or in addition, use these values automatically to determine a correct imaging plane from a series of planes that are all compatible to control electronics and an image processor of an imaging system during execution.

An ASID and the methods described above can find application in a wide range of applications, including conventional X-rays, for chest X-rays, for X-ray mammography, for X-ray tomography, for computerized tomography, for spiral computerized tomography, for X-ray bone densiometry, for γ-ray nuclear radiography, for gamma cameras for single photon emission computerised tomography (SPECT), for positron emission tomography (PET), for X-ray dental imaging, for X-ray panoramic dental imaging, for β-ray imaging using isotopes for DNA, RNA and protein sequencing, hybridization in situ, hybridization of DNA, RNA and protein isolated or integrated and generally for β-ray imaging and autoradiography using chromatography and polymerars chain reaction, for X-ray and γ-ray imaging in product quality control, for non-destructive testing and monitoring in realtime and online, and for security control systems.

Examples of the energies used in various of the applications mentioned above are: mammography (X-rays 10keV-50keV), tomography (X-rays 20keV-100keV), γ cameras (X-rays > 100keV), X-ray dental imaging (X-rays 40keV-100keV) X-ray product quality control (20keV-200keV), X-ray imaging in security systems (X-rays 60-120keV) DNA sequencing, hybridization in situ and hybridization on DNA isolated or integrated with β-ray isotopes 3H (18keV), 14C (155keV), 35S (170keV), 33P (250keV), 32P (1700keV).

It will be appreciated that the size of the pixel cells and the number of pixel cells which can be implemented on a single semiconductor detector will depend on the particular semiconductor integration technology used. Thus, although particular examples of sizes and component values have been given, the invention is not limited thereto and is intended to include changes in those dimensions and values as are possible with current such technology and will be possible with future technology. Also, it will be appreciated that the actual circuits shown, for example the pixel circuit 20 shown in Figures 2, 8 and 11 the connection lines and control circuitry illustrated in Figures 3, 4 and 9, are merely examples of possible circuits and that many modifications and additions are possible within the scope of the invention.

CLAIMS

1. An imaging device for imaging radiation, said imaging device comprising an array of pixel cells having a semiconductor substrate including an array of pixel detectors which generate charge in response to incident radiation and a corresponding array of pixel circuits, each pixel circuit being associated with a respective pixel detector for accumulating charge resulting from radiation incident on said pixel detector, said pixel circuits being individually addressable and comprising circuitry for accumulating charge from successive radiation hits on the respective pixel detectors.

2. An imaging device according to claim 1, wherein each pixel circuit comprises a charge storage device for accumulating charge.

3. An imaging device according to claim 2, wherein each pixel circuit comprises at least two transistors, a first transistor acting as said charge storage device and a second transistor acting as a readout switch, being responsive to an enable signal to connect said first transistor to an output line for outputting any accumulated charge.

4. An imaging device according to claim 3, wherein said transistors are field effect transistors.

5. An imaging device according to claim 4, wherein the FET capacitance of the first transistor substantially forms the input node capacitance of the pixel circuit.

6. An imaging device according to any one of claims 2 to 4, wherein each pixel circuit comprises a further field effect transistor responsive to a reset signal to reset said charge storage device.

7. An imaging device according to any one of claims 2 to 4, wherein the pixel circuit comprises overload protection circuitry, preferably diode overload discharge path means.

8. An imaging device according to any one of the preceding claims, wherein the charge value accumulated in a pixel circuit is output from a pixel circuit as a current value.

9. An imaging device according to any one of the preceding claims, wherein said pixel cell size is of the order of or less than 1mm across, preferably approximately 350μm across.

10. An imaging device according to any one of claims 1 to 9, wherein said pixel cell size is approximately 150μm across or less, preferably approximately 50μm across or less and more preferably approximately 10μm across.

11. An imaging device according to any one of the preceding claims, wherein said substrate is between 200μm and 3mm thick.

12. An imaging device according to any one of the preceding claims, wherein said pixel circuits are integral to said substrate and aligned with the corresponding pixel detectors.

13. An imaging device according to any one of claims 1 to 11, wherein said pixel circuits are formed in a further substrate, said further substrate incorporating said pixel circuits being coupled to said substrate incorporating said pixel detectors, with each pixel circuit being aligned with and being coupled to the corresponding pixel detector.

14. An imaging device according to any one of the preceding claims wherein said array comprises a single row of pixel detectors and associated pixel circuits forming a slit-shaped imaging device or a plurality of rows of pixel detectors and associated pixel circuits forming a slot-shaped imaging device.

15. An imaging device according to claim 14 wherein said pixel circuits for respective pixel detectors are laterally adjacent to the corresponding pixel detectors.

16. An imaging device according to any one of the preceding claims in combination with control electronics including addressing logic for addressing individual pixel circuits for reading accumulated charge from said pixel circuits and selectively resetting said pixel circuits.

17. An imaging device according to claim 16, wherein said addressing logic comprises means for connecting output lines of said pixels circuits to an output of said imaging device, means for supplying read enable signals to read enable inputs of said pixel circuits and means for supplying reset signals to reset inputs of said pixel circuits.

18. An imaging device according to claim 17 wherein said means for connecting output lines comprises a shift register for sequentially connecting output lines of said pixel circuits for respective columns of pixels to said output of said imaging device.

19. An imaging device according to claim 17 or claim 18 wherein said means for supplying read enable signals comprises a shift register for sequentially supplying read enable signals to read enable inputs of said pixel circuits for respective rows of pixels.

20. An imaging device according to any one of claims 16 to 19 wherein said means for supplying reset signals comprises a shift register for sequentially supplying reset signals to reset inputs of said pixel circuits for respective rows of pixels.

21. An imaging device according to any one of claims 16 to 20, wherein said control electronics includes an analogue to digital converter for converting an analogue charge value from a said pixel circuit into a digital charge value.

22. An imaging device according to any one of claims 16 to 21, wherein at least part of said control electronics is integrated into a semiconductor substrate on which said pixel circuits are integrated.

23. An imaging device according to any one of the preceding claims, wherein the semiconductor substrate is made of a material selected

from: CdZnTe, CdTe, HgI_2, GaAs, Ge, TlBr and Si.

24. An imaging system comprising an imaging device according to any one of claims 21 to 23, said imaging system comprising an image processor connected to said control electronics for processing said digital charge values from respective pixel circuits to form an image for display on a display device.

25. An imaging system according to claim 24, wherein said processor determines maximum and minimum charge values for pixels for display, assigns extreme grey scale or colour values to said maximum and minimum charge values and allocates grey scale or colour values to an individual pixel according to a sliding scale between said extreme values in dependence upon the charge value for said pixel.

26. An imaging system according to claim 25, wherein said grey scale or colour values are allocated in accordance with the following formula:

$$\text{Grey scale value of pixel } i = \text{Min}_{grey} + \frac{(i_{charge}-\text{Min}_{charge})}{(\text{Max}_{charge}-\text{Min}_{charge})} \times (\text{Max}_{grey}-\text{Min}_{grey})$$

27. An imaging system comprising a plurality of imaging devices according to any one of claims 1 to 23 tiled together to form a mosaic.

28. An imaging system according to claim 27 wherein said mosaic comprises a plurality of columns of tiled imaging devices, said imaging devices of adjacent columns being offset in the column direction.

29. An imaging system according to claim 27 or claim 28 comprising means for stepping said imaging device to accumulate an image over a complete image area.

30. An imaging system according to claim 27 or claim 28 comprising two imaging surfaces, each comprising a mosaic of imaging devices, said imaging surfaces being arranged substantially parallel to one another

and spaced from one another with an object to be imaged between said surfaces, the mosaics being offset laterally with respect to one another to give substantially complete imaging of said object.

31. An imaging system comprising a plurality of imaging devices according to any one of claims 1 to 23 wherein said imaging devices are arranged substantially tangentially around the periphery of a ring or part-ring to encircle or partially encircle a slice of an object to be imaged by for example a computerized tomography technique.

32. An imaging system according to claim 31, wherein said imaging devices are arranged substantially tangentially around the periphery of a plurality of rings or part-rings displaced from one another in the direction forming a common axis of said rings or part-rings.

33. An imaging system comprising a plurality of imaging devices according to any one of claims 1 to 23 tiled together to form a mosaic matching the area and shape of an object to be imaged.

34. An imaging system comprising a plurality of imaging devices according to any one of claims 1 to 23 tiled together to form a mosaic surrounding part or all of an object to be imaged.

35. An imaging system according to any one of claims 27 to 34 wherein respective image outputs of a plurality of tiled imaging devices are connected to a common multiplexer, the output of which multiplexer is connected to a common analogue to digital converter.

36. An imaging device according to claim 35, wherein the output of said multiplexer comprises current values representative of accumulated charge from said pixel circuits.

37. An imaging system according to any one of claims 24 to 36, wherein individual pixel circuits are addressed for reading accumulated charge at a rate to optimise the resolution of an analogue to digital converter for converting analogue accumulated charge values into digital values.

38. An imaging system according to any one of claims 24 to 37, wherein multiple image frames are accumulated, either at an analogue to digital conversion stage, or subsequently at an image processing stage.

39. An imaging system comprising one or more slit- or slot-shaped imaging device(s) according to claim 14 or claim 15 and means for relative movement between said slit- or slot-shaped imaging device(s) and an object to be imaged in a direction transversely to a longitudinal axis of said imaging device(s) for accumulating a complete image over an imaging area.

40. A method of operating an imaging system according to claim 39 comprising providing relative movement between said slit- or slot-shaped imaging device(s) and an object to be imaged in said transverse direction and reading accumulated charge from said pixel circuits of said slit- or slot-shaped imaging device(s) at a rate corresponding to said movement by half or less than half of the pixel size in the direction of motion.

41. A method of operating an imaging system comprising one or more slit- or slot-shaped imaging devices according to claim 14 or claim 15 comprising minimising the effect of scattered radiation by optimising the relationship between the following parameters: the distance between a radiation source and an object to be imaged; the distance between the object to be imaged and the slit- or slot-shaped imaging device(s); and the width of the slit- or slot-shaped imaging device(s).

42. A method for imaging accumulated values corresponding to respective pixel positions within a pixel array, such as, for example, charge values accumulated for respective pixel positions of an imaging device as defined in any one claims 1 to 23, said method comprising:

- determining maximum and minimum accumulated values for pixels within an area of said pixel array to be imaged;
- assigning grey scale or colour values at extremes of a grey or colour scale to be imaged to said maximum and minimum accumulated values; and
- assigning grey scale or colour values to said accumulated

values for individual pixels scaled in accordance with said extreme values; and

- imaging said assigned grey scale or colour values at respective image pixel positions.

43. A method for automatically detecting and eliminating detected pixel value representative of radiation incident on a pixel detector of an imaging device, for example an imaging device according to any one of claims 1 to 23, said method comprising:

- comparing said detected pixel value to a threshold value related to a minimum detected charge value expected for directly incident radiation; and

- discarding detected pixel values less than said threshold value.

44. A method of automatically optimising imaging using, for example, an imaging system according to any one of claims 24 to 39 for different imaging applications where incident radiation leaves a different electrical signal in a pixel detector of a semiconductor substrat dependent on a semiconductor material or compound used and an energy and a type of incident radiation, said method comprising:

- determining an expected best resolution using a centre of gravity technique;

- determining an expected efficiency as a function of radiation type and energy; and

- either determining a pixel size and thickness as a function of a selected radiation type and energy and a selected semiconductor material or compound or determining the best semiconductor choice for a given radiation type and energy as a function of the achieved resolution and efficiency.

45. A method according to claim 44 comprising automatically selecting an imaging device having said determined pixel size and thickness.

46. A method for performing real time imaging of an organic or inorganic object, said method comprising:

- irradiating said object using a radiation source that produces X-

rays, γ-rays, β-rays or α-rays;

- detecting at a semiconductor imaging plane or planes of an imaging device according to any one of claims 1 to 23 unabsorbed radiation or radiation that is emitted from selected areas of said object, whereby the amount of charge resulting from radiation incident successively on respective pixel detectors of said imaging device is accumulated in respective pixel circuits;
- addressing said pixel circuits individually for reading out accumulated charge;
- processing said read out charge to provide image pixel data; and
- displaying said image pixel data.

47. A method of operating an imaging device according to any one of claims 1 to 23 or an imaging system according to any one of claims 24 to 39, the method comprising

reading the accumulated charge from individual pixel circuits at a rate to optimise the resolution of an analogue to digital converter for converting analogue accumulated charge values into digital values.

48. Use of an imaging device according to any one of claims 1 to 23 or of an imaging system according to any one of claims 24 to 39 for conventional X-rays, for chest X-rays, for X-ray mammography, for X-ray tomography, for computerized tomography, for spiral computerized tomography, for X-ray bone densiometry, for γ-ray nuclear radiography, for gamma cameras for single photon emission computerised tomography (SPECT), for positron emission tomography (PET), for X-ray dental imaging, for X-ray panoramic dental imaging, for β-ray imaging using isotopes for DNA, RNA and protein sequencing, hybridization in situ, hybridization of DNA, RNA and protein isolated or integrated and generally for β-ray imaging and autoradiography using chromatography and polymerars chain reaction, for X-ray and γ-ray imaging in product quality control, for non-destructive testing and monitoring in realtime and online, and for security control systems.

49. An imaging device substantially as hereinbefore described with reference to the accompanying drawings.

50. An imaging system substantially as hereinbefore described with reference to the accompanying drawings.

51. An imaging method substantially as hereinbefore described with reference to the accompanying drawings.

57

Patents Act 1977
Examiner's report to the Comptroller under Section 17
(The Search report)

Application number
GB 9508294.7

Relevant Technical Fields

(i) UK Cl (Ed.N) H1K (KECCB, KECCX); H4F (FCC, FGXX)

(ii) Int Cl (Ed.6) H01L 27/148; H04N 1/10; 5/14

Search Examiner
R C HRADSKY

Date of completion of Search
11 AUGUST 1995

Databases (see below)
(i) UK Patent Office collections of GB, EP, WO and US patent specifications.

(ii) ONLINE: WPI

Documents considered relevant following a search in respect of Claims :-
1-41, 46-48

Categories of documents

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Category	Identity of document and relevant passages		Relevant to claim(s)
X	GB 2262383 A	(SONY) whole document	1, 46, 48
X	GB 2249430 A	(MITSUBISHI) whole document	1, 46, 48
X	WO 91/10170 A1	(MFG SCIENCES) whole document	1, 46, 48

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